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C1

sulfonic acid; bissulfopropyl disulfide; 3-(benzthiazolyl-s-thio)propyl sulfonic acid; and 3-mercaptopropane-1-sulfonate.

REMARKS

Non-elected claims 28-123 have been cancelled without prejudice, and claims 138 and 139 have been amended to obviate a non-substantive objection. No new matter has been added by virtue of the amendments.

The undersigned affirms the election to the Restriction Requirement as specified in the Office.

It is believed the amendments made herein obviate the objection to claims 138 and 139.

Claims 124-138 and 141-153 were rejected under 35 U.S.C. 103 over Creutz (U.S. Patent 3,770,598) in view of Sonnenberg (U.S. Patent 5,252,196).

Claims 139-140 were rejected under 35 U.S.C. 103 over Creutz (U.S. Patent 3,770,598) and Sonnenberg (U.S. Patent 5,252,196) and further in view of Dahms (U.S. Patent 5,433,840).

For the sake of brevity, the two rejections are addressed in combination. Such a combined response is considered appropriate because, *inter alia*, each rejection relies on the Creutz and Sonnenberg documents as primary citations.

Each of the rejections is traversed.

In the Office Action, it is specifically acknowledged that the cited documents do not disclose electroplating on a microchip wafer. The position is nevertheless taken that plating on such a substrate would have been obvious. In particular, the following is stated at page 7 of the Office Action:

> [I]t would have been obvious and within the ordinary skill in the art at the time the invention was made to have used semiconductor microchip wafers instead of printed circuit boards as taught by Sonnenberg et al. because both substrates are concerned with electroplating interconnects to conduct electricity, with the only difference being the scale of the interconnect size. Accordingly, one of ordinary skill in the art would have used the teachings of Creutz and Sonnenberg et al. as a starting point to electrodeposit metal on microchip wafers.

Respectfully, that position does not withstand scrutiny. Persons skilled in the art recognize that plating copper on a microelectronic wafer is considerably more difficult, and posses unique issues, relative to plating copper on a printed circuit board.

This is made clear in, for instance, U.S. Patent 6,290,833, copy enclosed. Thus, at column 2, lines 35-39 of that patent, the following is reported (bold emphasis added):

> Despite the advantageous properties of copper, **it has not been as widely used as an interconnect material as one would expect. This is due, at least in part, to the difficulty of depositing copper metallization** and, further, due to the need for the presence of barrier layer materials.

U.S. Patent 6,297,154, copy enclosed, reports the following at column 2, lines 33-37 (bold emphasis added):

> As noted in U.S. Pat. No. 5,627,102 to Shrinriki et al., **one problem associated with the formation of metal interconnects is that voids form in the metal filling of the recess**. Such faulty fill-up leads to a failure to establish a sound electrical contact.

U.S. Patent 6,171,960, reports the following at column 1, lines 10-27 (bold emphasis added):

> The fabrication of deep submicron ultra scale integrated (ULSI) circuits requires long interconnects having small connects and small cross-sections. To achieve the above objective, the preferred interconnect material is copper. Copper provides a number of advantages for wiring applications including low resistivity and a high melting point.
>
> At present, aluminum is the material used in fabricating interconnects on most integrated circuits. This invention seeks to replace the aluminum with copper in the fabrication of advanced circuits and ultra-fast logic devices.
>
> **Many problems, however, are encountered in fabricating interconnects with copper.** Some of the major difficulties include: (a) copper oxidizes easily at low temperatures; (2) copper has poor adhesion to substrates; (3) copper diffuses into silicon dioxide and other dielectric material used in micro-circuitry; and (4) copper requires a high temperature for reactive ion etching.

Thus, the understanding of the art was directly contrary to the position advanced in the Office Action, i.e. the art recognized that unique issues were associated with plating copper on semiconductor substrates. Accordingly, the skilled worker would not have considered it at all obvious to plate semiconductor microchip wafer substrates with a composition reported for plating on printed circuit boards.

Additionally, the position advanced in the Office Action is unsubstantiated and therefore the rejection is improper. See Section 2143.03 of the annual of Patent Examining Procedure ("To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art.").

Moreover, while Applicants fully believe that a prima facie case of obviousness has not been presented by the cited documents, it is also believed that the comparative data of record effectively rebuts any prima facie case that may be contended to exist.

Attention is directed to the comparative results detailed at Examples 2 and 3 of the application. In Example 2, using a copper electroplating composition of the invention having a brightener concentration of 2.4 mg/l, semiconductor microvias were filled with copper deposits having no defects as determined by focussed beam examination. In comparative Example 3, a copper electroplating composition having a brightener concentration of 0.35 mg/l produced a copper deposit with defects in semiconductor microvias.

In view thereof, reconsideration and withdrawal of the rejections are requested

It is believed the present application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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Boston, MA 02209
(617) 439-4444

VERSION WITH CHANGES MARKED

139. (amended) The method [article] of claim 137 wherein the one or more brighteners correspond to one of the following formulae:

XO_3S-R-SH

XO_3S-R-S-S-R-SO_3X

XO_3S-Ar-S-S-Ar-SO_3X

wherein R is optionally substituted alkyl; Ar is optionally substituted aryl; and X is a counter ion.

139. (amended) The method [article] of claim 137 wherein the one or more brighteners are selected from the group consisting of n,n-dimethyl-dithiocarbamic acid-(3-sulfopropyl)ester; 3-mercapto-propylsulfonic acid; carbonic acid-dithio-o-ethyl-s-ester with 3-mercapto-1-propane sulfonic acid; bissulfopropyl disulfide; 3-(benzthiazolyl-s-thio)propyl sulfonic acid; and 3-mercaptopropane-1-sulfonate.

US006290833B1

(12) **United States Patent**
Chen

(10) **Patent No.: US 6,290,833 B1**
(45) **Date of Patent: Sep. 18, 2001**

(54) **METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORKPIECE**

(75) Inventor: **Linlin Chen**, Kalispell, MT (US)

(73) Assignee: **Semitool, Inc.**, Kalispell, MT (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/387,033**

(22) Filed: **Aug. 31, 1999**

Related U.S. Application Data

(63) Continuation of application No. PCT/US99/06306, filed on Mar. 22, 1999, which is a continuation of application No. 09/045,245, filed on Mar. 20, 1998, now Pat. No. 6,197,181.
(60) Provisional application No. 60/085,675, filed on May 15, 1998.

(51) **Int. Cl.**[7] **C25D 5/10**
(52) **U.S. Cl.** **205/182**; 205/170; 205/296
(58) **Field of Search** 205/291, 296, 205/123, 125, 157, 170, 182

(56) **References Cited**

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Primary Examiner—Kathryn Gorgos
Assistant Examiner—Wesley A. Nicolas
(74) *Attorney, Agent, or Firm*—Christensen O'Connor Johnson Kindness PLLC

(57) **ABSTRACT**

This invention employs a novel approach to the copper metallization of a workpiece, such as a semiconductor workpiece. In accordance with the invention, an alkaline electrolytic copper bath is used to electroplate copper onto a seed layer, electroplate copper directly onto a barrier layer material, or enhance an ultra-thin copper seed layer which has been deposited on the barrier layer using a deposition process such as PVD. The resulting copper layer provides an excellent conformal copper coating that fills trenches, vias, and other microstructures in the workpiece. When used for seed layer enhancement, the resulting copper seed layer provide an excellent conformal copper coating that allows the microstructures to be filled with a copper layer having good uniformity using electrochemical deposition techniques. Further, copper layers that are electroplated in the disclosed manner exhibit low sheet resistance and are readily annealed at low temperatures.

27 Claims, 10 Drawing Sheets

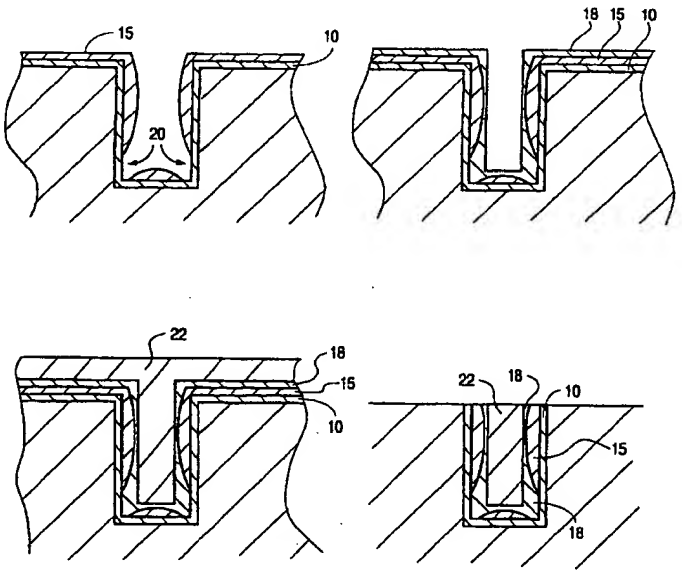


Fig. 1

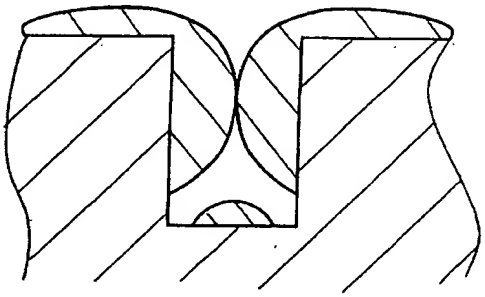


Fig. 2A

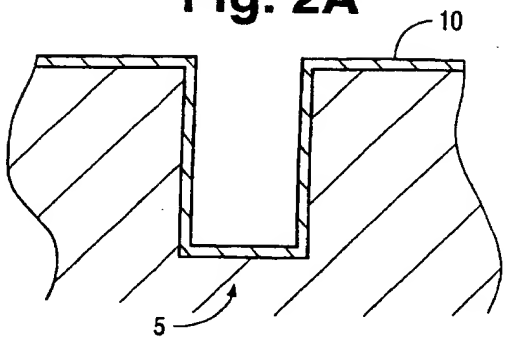


Fig. 2B

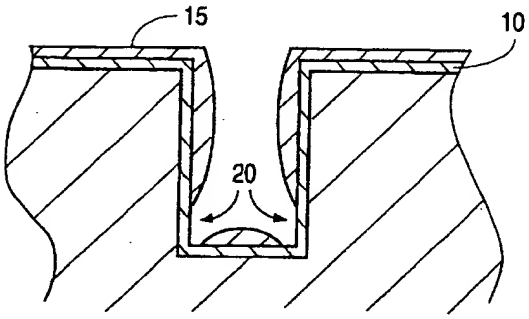


Fig. 2C

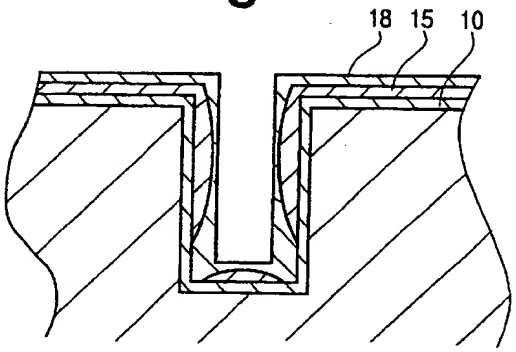


Fig. 2D

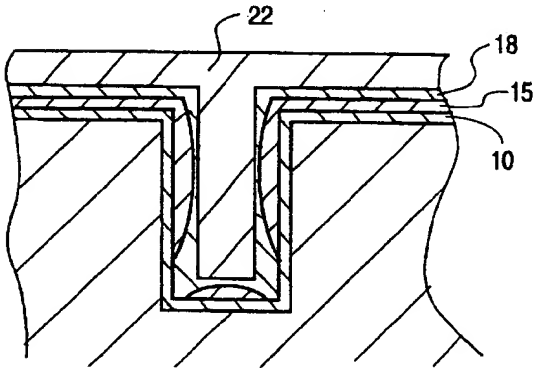


Fig. 2E

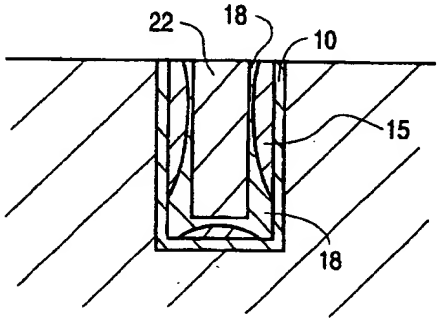
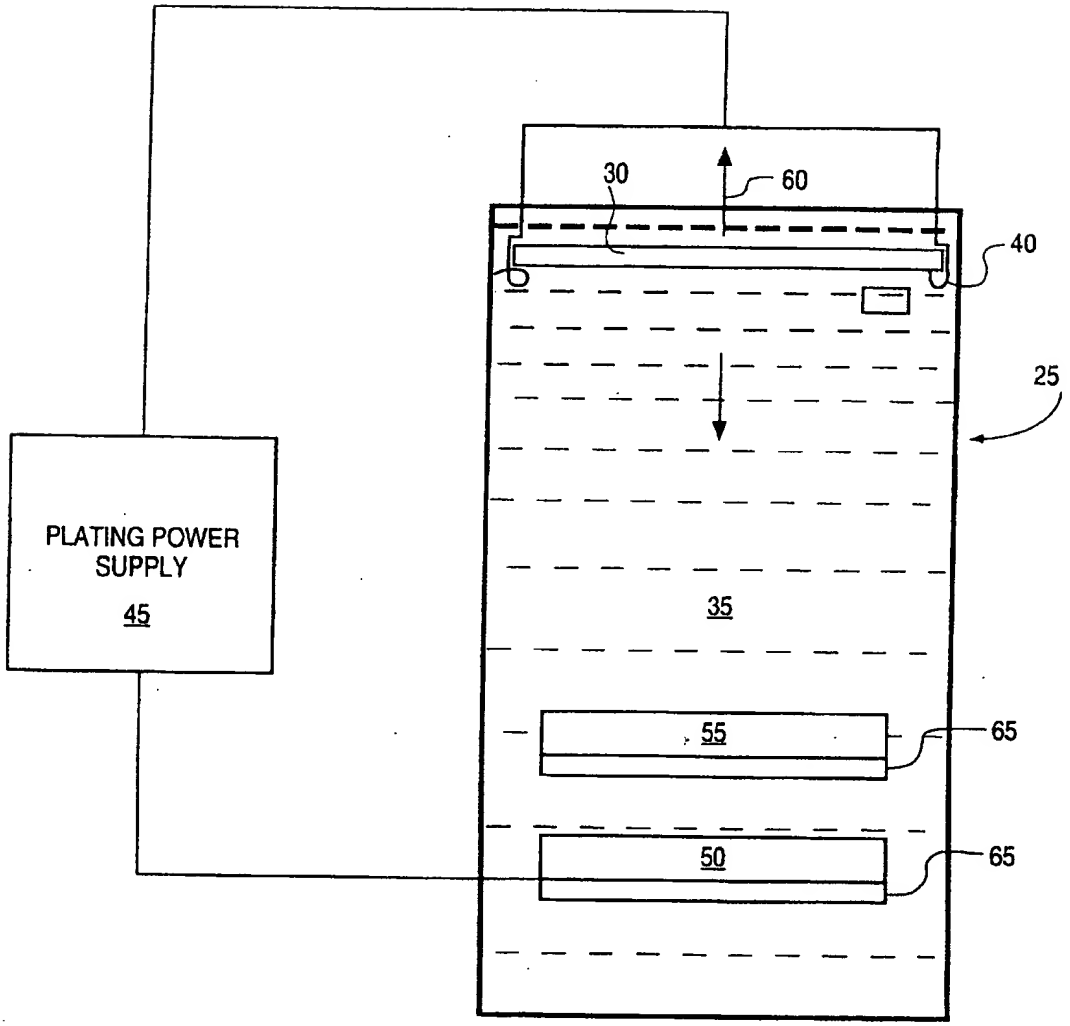


Fig. 3



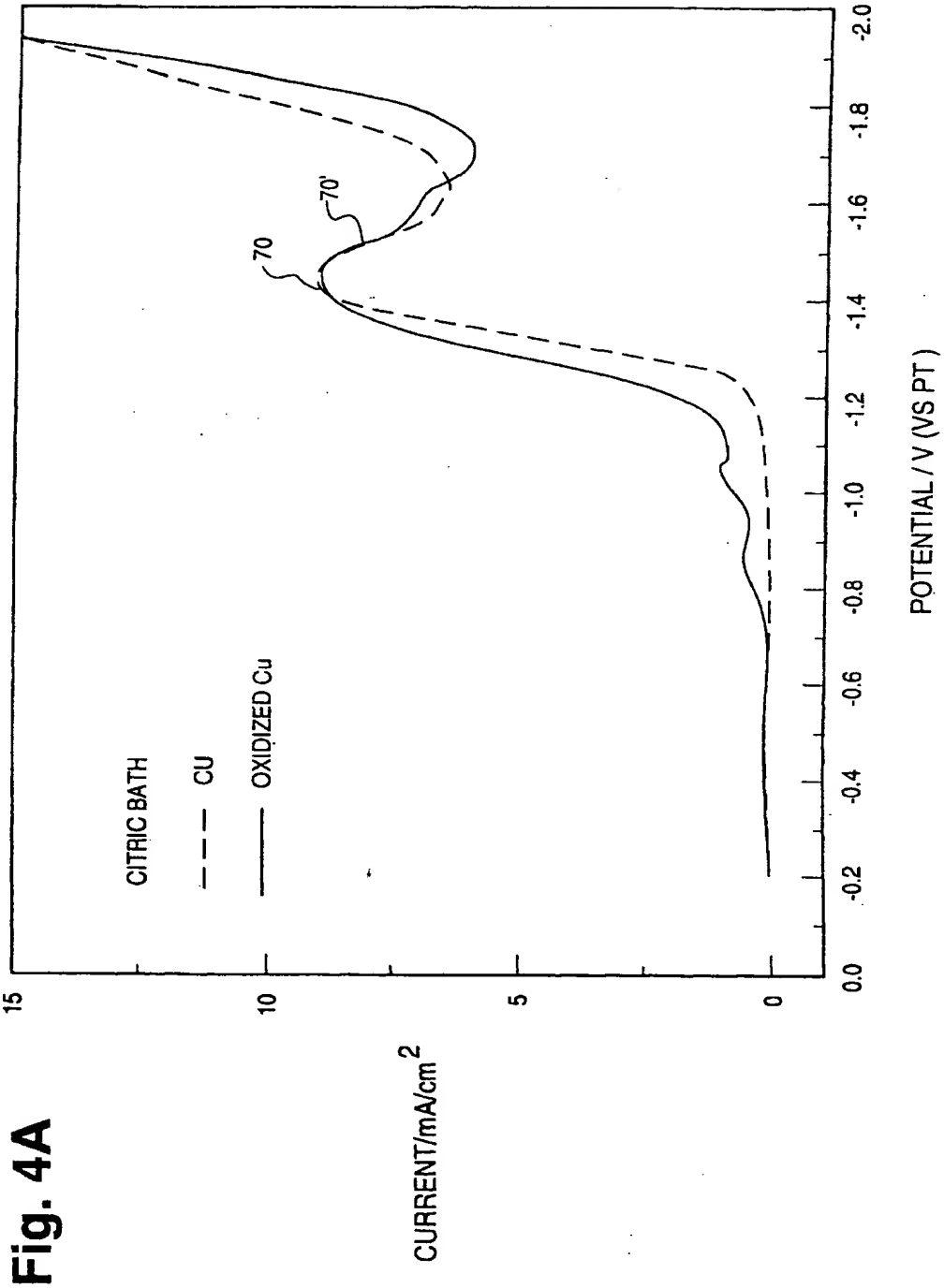

CITRIC BATH
CU
OXIDIZED Cu
70
70'
CURRENT/mA/cm^2
15
10
5
0
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
-1.4
-1.6
-1.8
-2.0
POTENTIAL / V (VS PT)

Fig. 4A

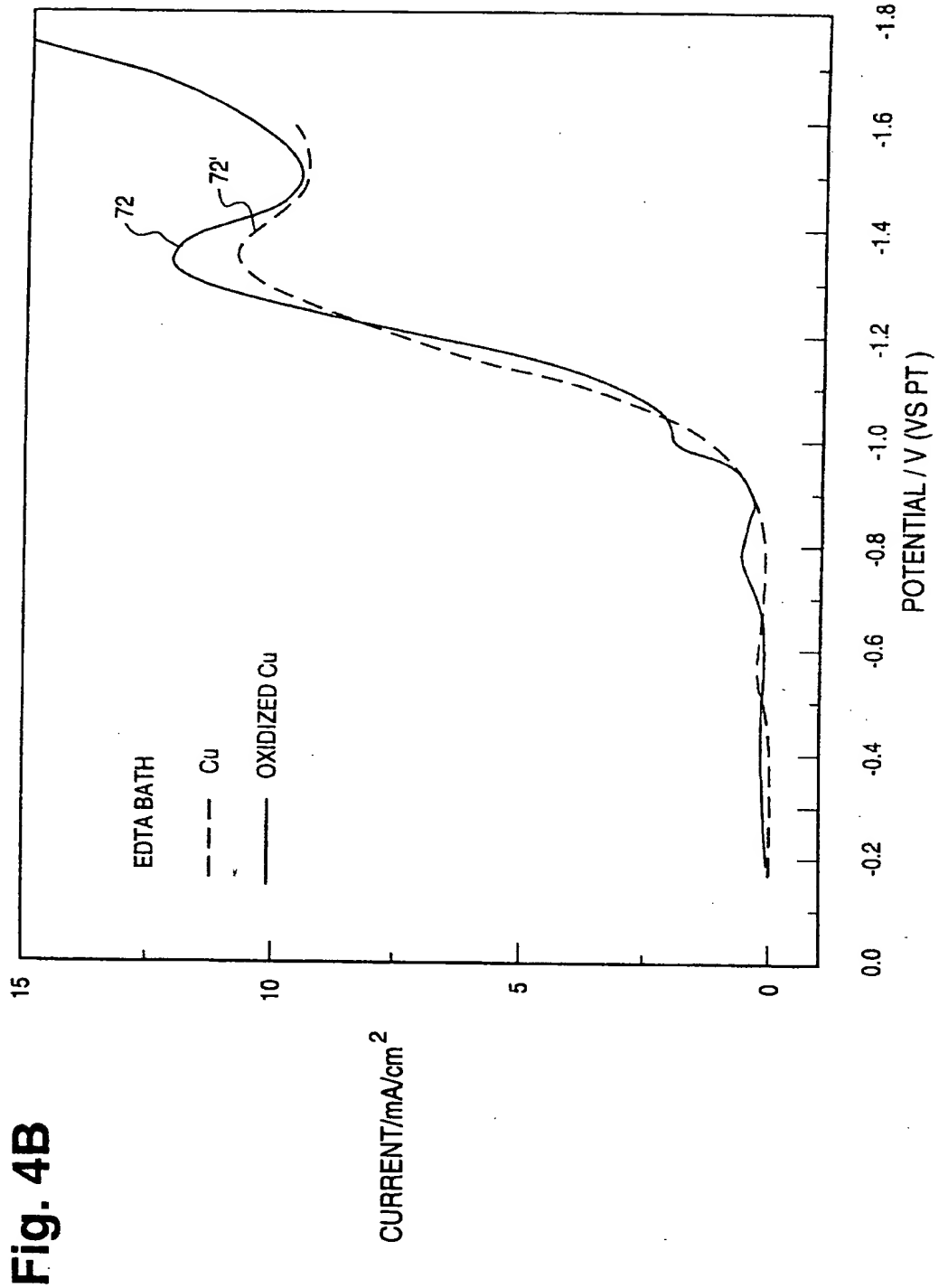

EDTA BATH
Cu
OXIDIZED Cu
72
72'
CURRENT/mA/cm^2
15
10
5
0
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
-1.4
-1.6
-1.8
POTENTIAL / V (VS PT)

Fig. 4B

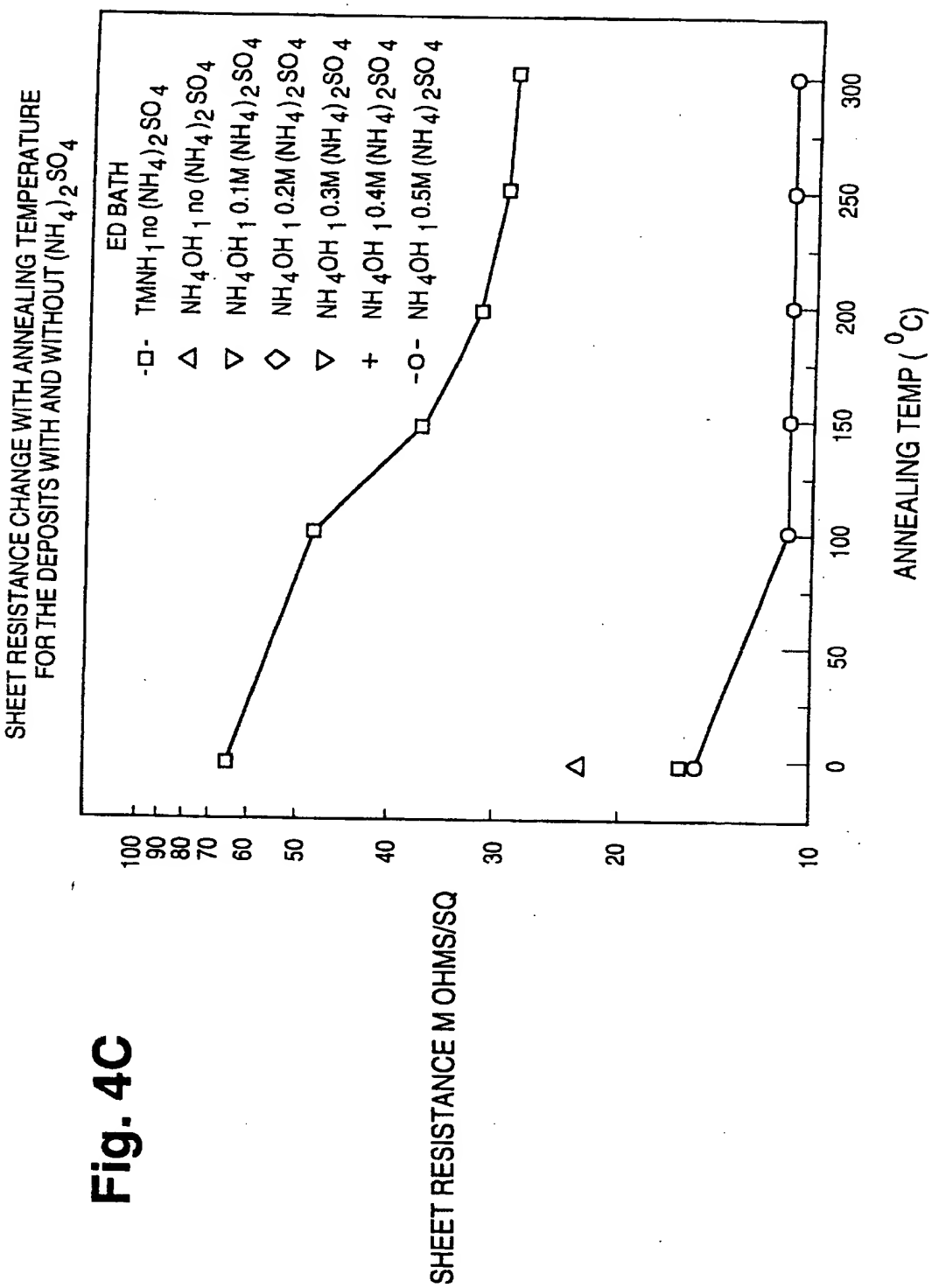

SHEET RESISTANCE CHANGE WITH ANNEALING TEMPERATURE
FOR THE DEPOSITS WITH AND WITHOUT $(NH_4)_2SO_4$
ED BATH
-□- $TMNH_1$ no $(NH_4)_2SO_4$
△ NH_4OH_1 no $(NH_4)_2SO_4$
▽ NH_4OH_1 0.1M $(NH_4)_2SO_4$
◇ NH_4OH_1 0.2M $(NH_4)_2SO_4$
▽ NH_4OH_1 0.3M $(NH_4)_2SO_4$
+ NH_4OH_1 0.4M $(NH_4)_2SO_4$
-○- NH_4OH_1 0.5M $(NH_4)_2SO_4$
SHEET RESISTANCE M OHMS/SQ
100
90
80
70
60
50
40
30
20
10
0
50
100
150
200
250
300
ANNEALING TEMP (^0C)

Fig. 4C

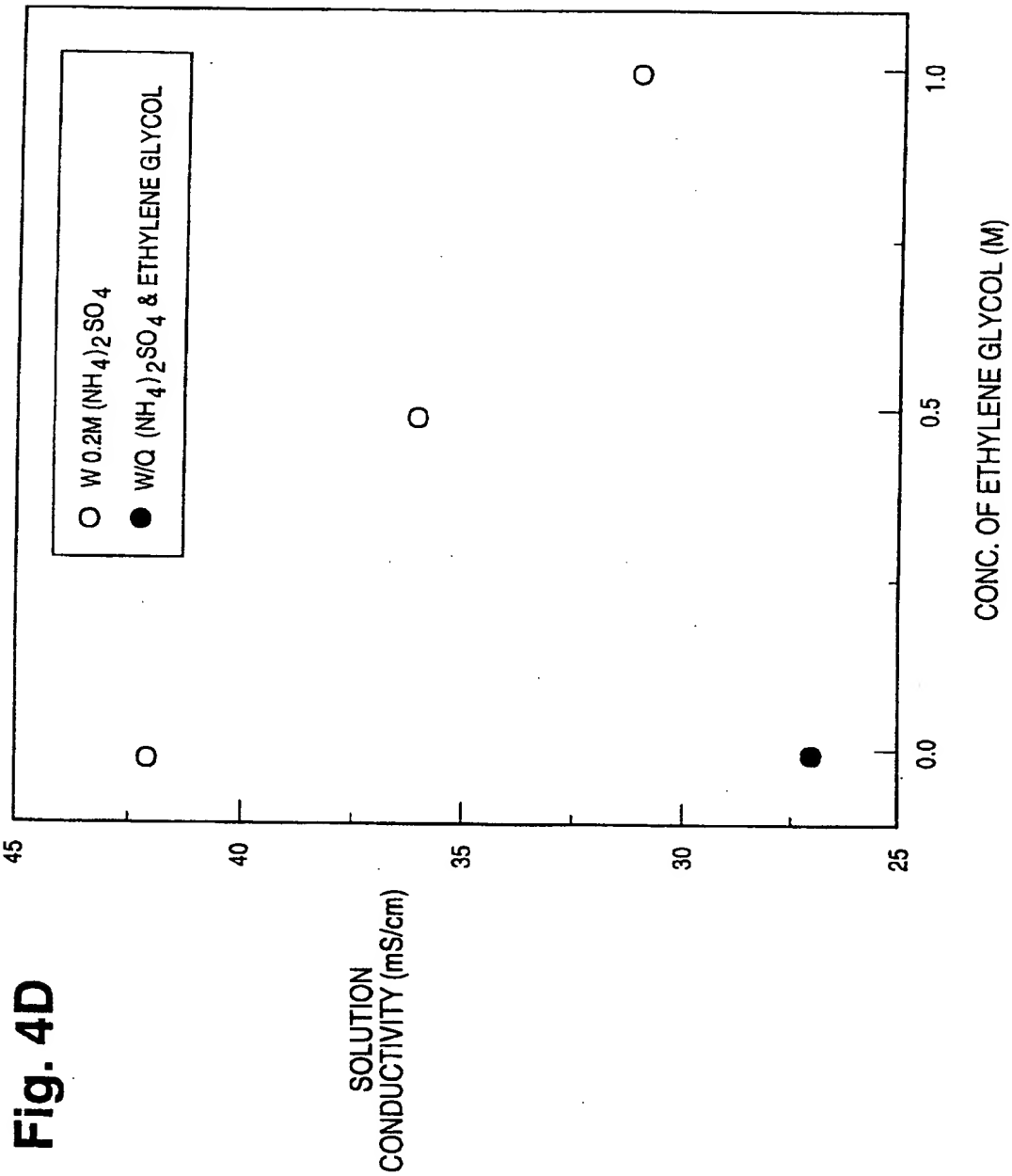

W 0.2M $(NH_4)_2SO_4$
W/O $(NH_4)_2SO_4$ & ETHYLENE GLYCOL
SOLUTION CONDUCTIVITY (mS/cm)
45
40
35
30
25
0.0
0.5
1.0
CONC. OF ETHYLENE GLYCOL (M)

Fig. 4D

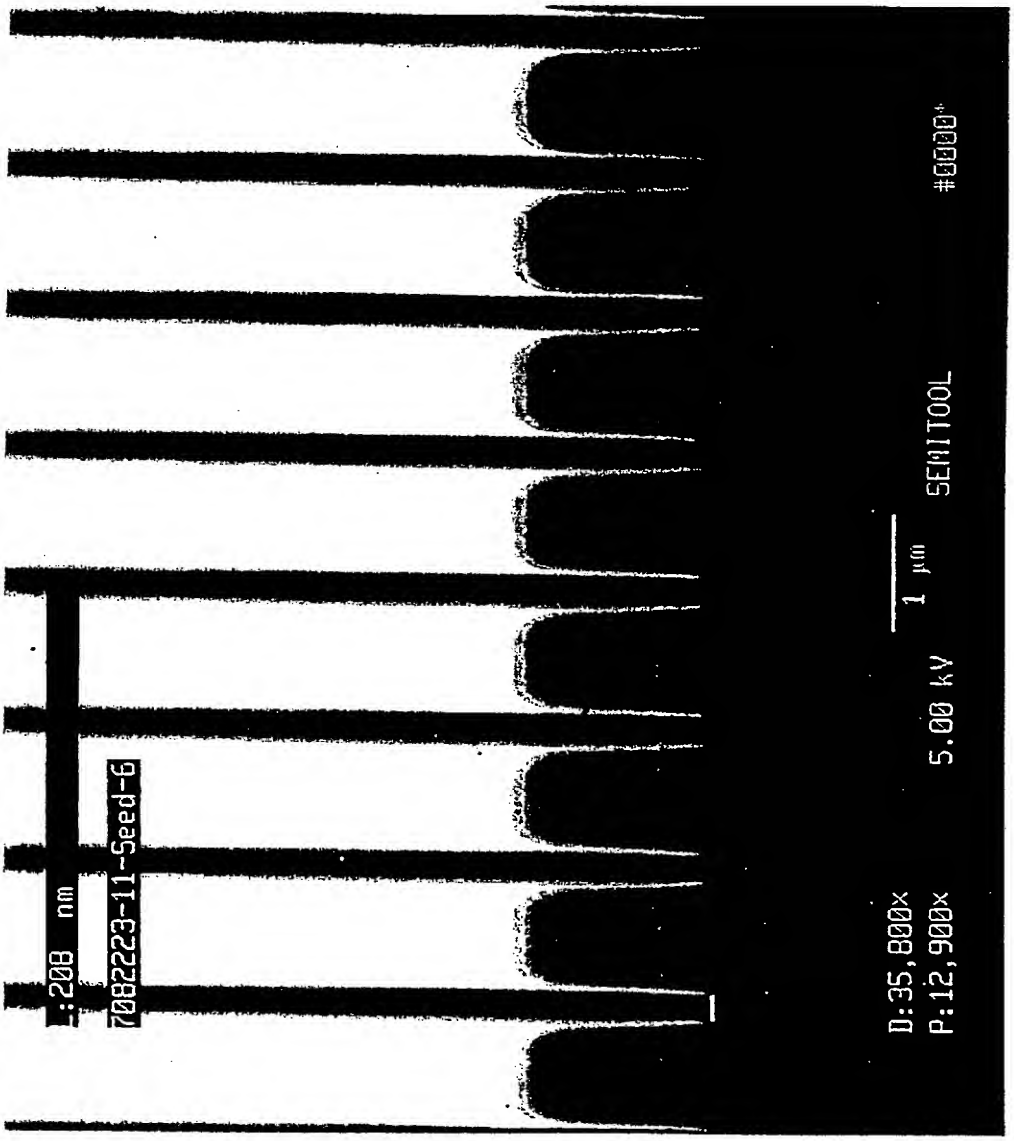

:200 nm
7082223-11-Seed-6
D:35,800x
P:12,900x
5.00 kV
1 μm
SEMITOOL
#0000

Fig. 5

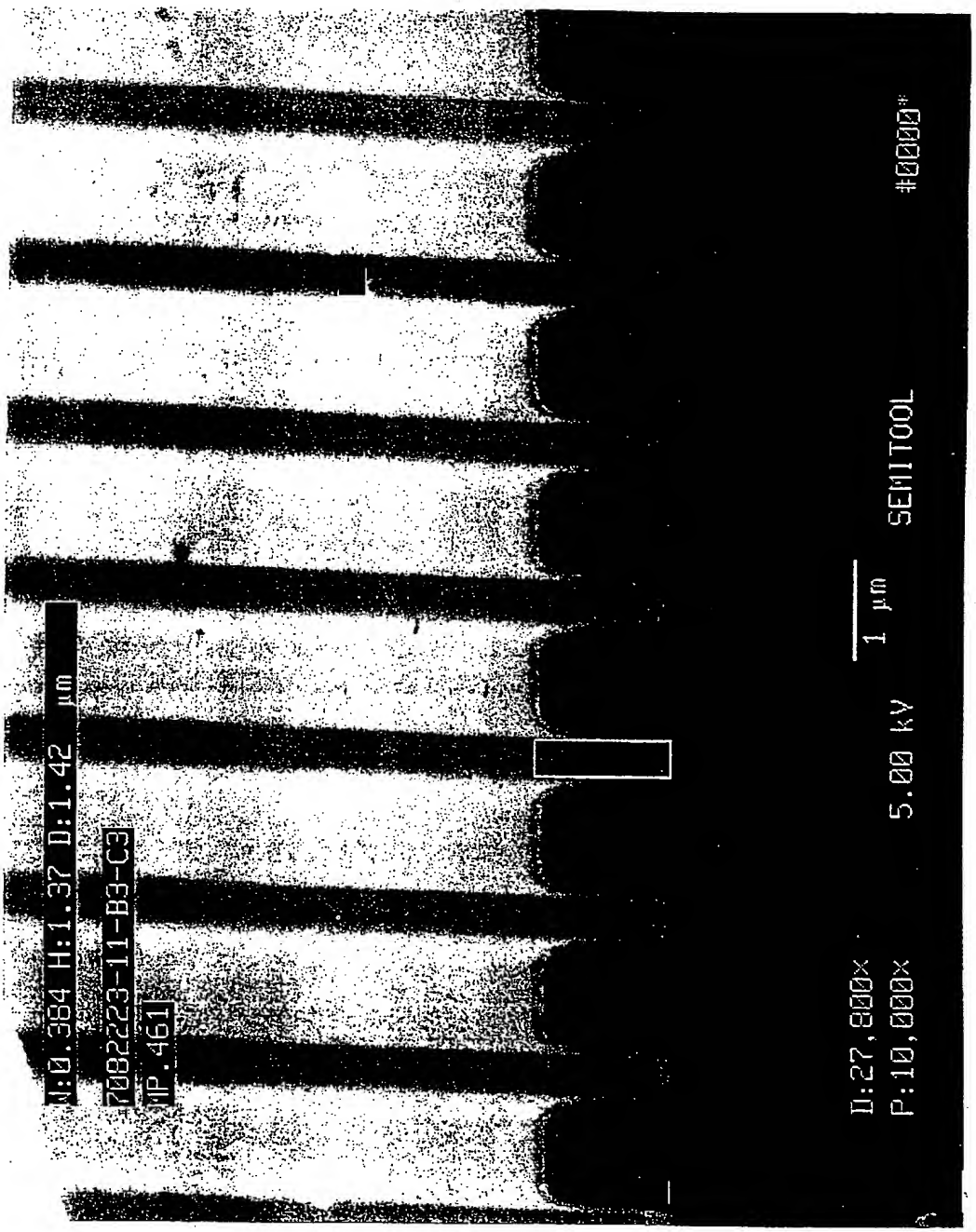

N:0.384 H:1.37 D:1.42 µm
7082223-11-B3-C3
MP.461
D:27,800×
P:10,000×
5.00 kV
1 µm
SEMITOOL
#0000

Fig. 6A

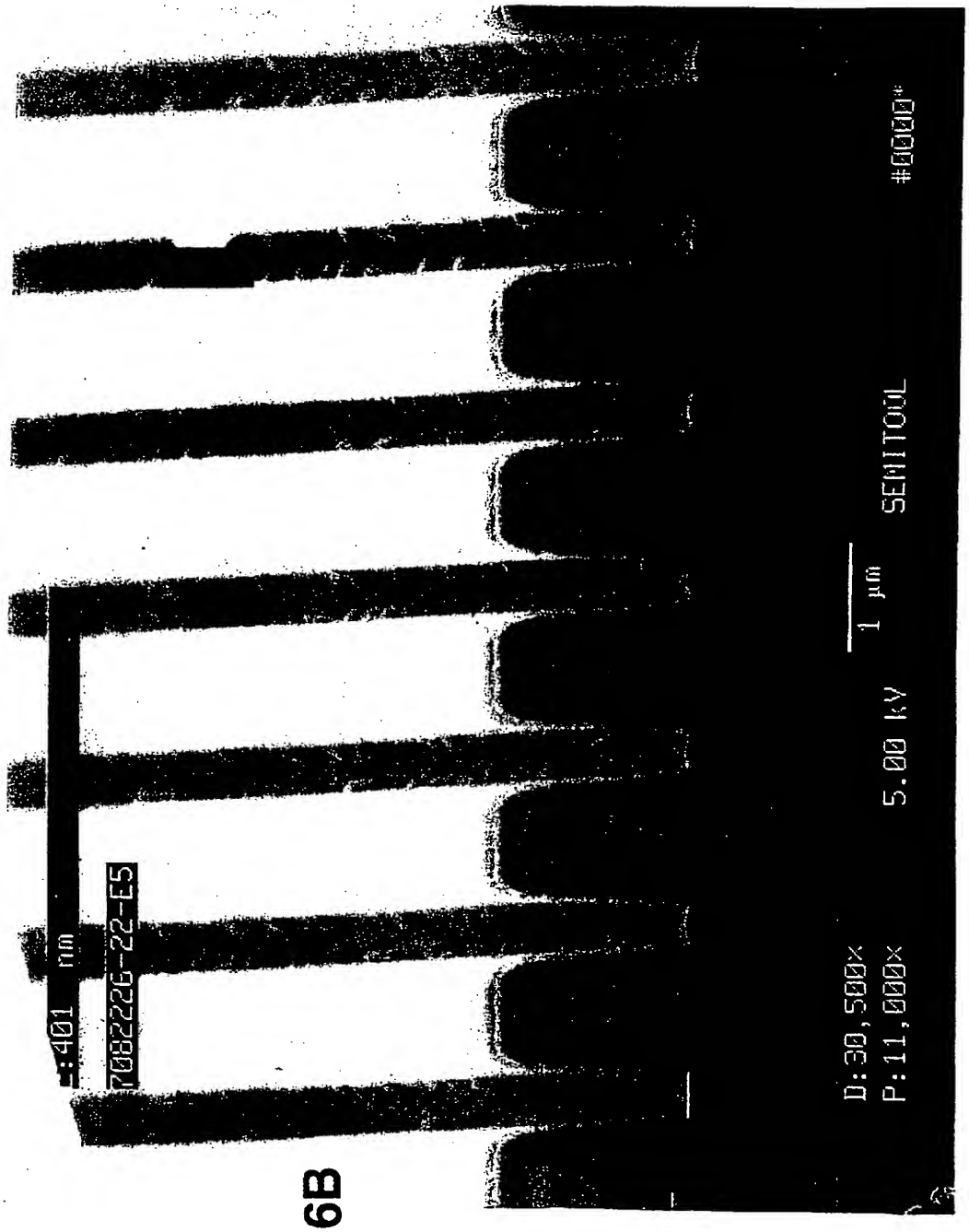
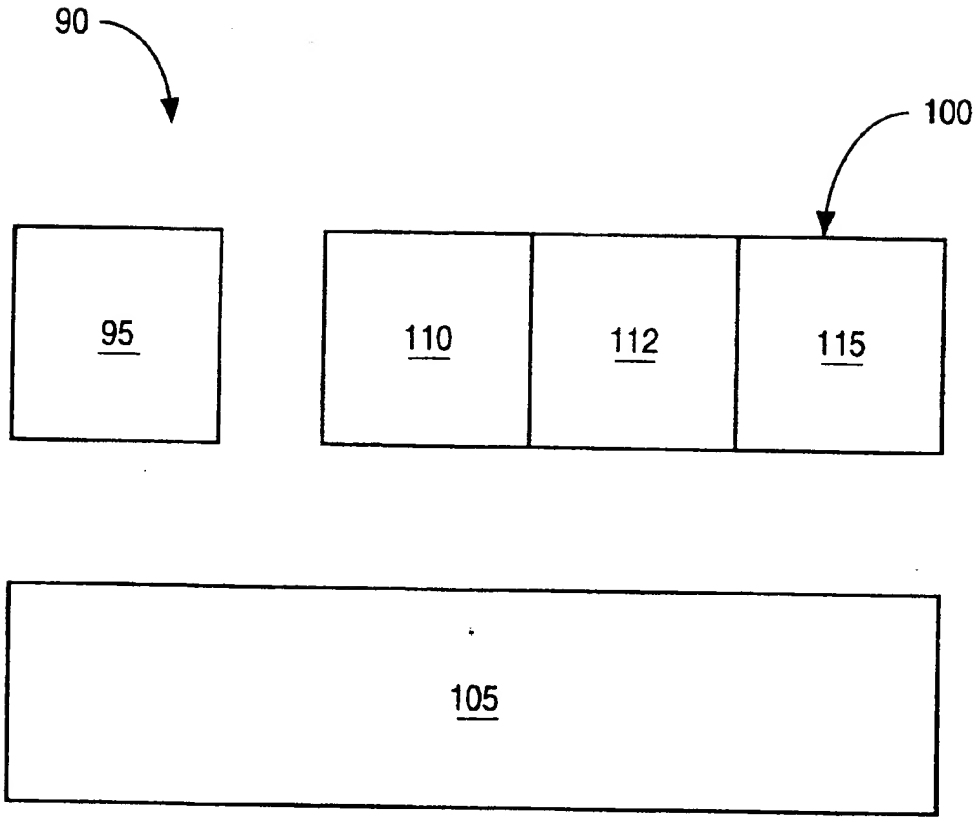


Fig. 6B

Fig. 7



METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORKPIECE

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation application of International PCT Patent Application No. PCT/US99/06306, designating the US, filed Mar. 22, 1999, entitled APPARATUS AND METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORKPIECE, which continuation U.S. patent application Ser. No. 09/045,245, filed Mar. 20, 1998, now U.S. Pat. No. 6,197,181, and U.S. patent application Ser. No. 60/085,675, filed May 15, 1998.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

BACKGROUND OF THE INVENTION

In the fabrication of microelectronic devices, application of one or more metallization layers is often an important step in the overall fabrication process. The metallization may be used in the formation of discrete microelectronic components, such as read/write heads, but it is more often used to interconnect components formed on a workpiece, such as a semiconductor workpiece. For example, such structures are used to interconnect the devices of an integrated circuit.

A basic understanding of certain terms used herein will assist the reader in understanding the disclosed subject matter. To this end, basic definitions of certain terms, as used in the present disclosure, are set forth below.

- Single Metallization Level is defined as a composite level of a workpiece that is exterior to the substrate. The composite level comprises one or more metal structures.
- Substrate is defined as a base layer of material over which one or more metallization levels are disposed. The substrate may be, for example, a semiconductor wafer, a ceramic block, etc.
- Workpiece is defined as an object that at least comprises a substrate, and may include further layers of material or manufactured components, such as one or more metallization levels, disposed on the substrate.

An integrated circuit is an interconnected ensemble of devices formed within a semiconductor material and within a dielectric material that overlies a surface of the semiconductor. Devices which may be formed within the semiconductor include MOS transistors, bipolar transistors, diodes and diffused resistors. Devices which may be formed within the dielectric include thin-film resistors and capacitors. Typically, more than 100 integrated circuit die (IC chips) are constructed on a single 8 inch diameter silicon wafer. The devices utilized in each dice are interconnected by conductor paths formed within the dielectric. Typically, two or more levels of conductor paths, with successive levels separated by a dielectric layer, are employed as interconnections. In current practice, an aluminum alloy and silicon oxide are typically used for, respectively, the conductor and dielectric.

Delays in propagation of electrical signals between devices on a single die limit the performance of integrated circuits. More particularly, these delays limit the speed at which an integrated circuit may process these electrical signals. Larger propagation delays reduce the speed at which the integrated circuit may process the electrical signals, while smaller propagation delays increase this speed. Accordingly, integrated circuit manufacturers seek ways in which to reduce the propagation delays.

For each interconnect path, signal propagation delay may be characterized by a time delay τ. See E. H. Stevens, *Interconnect Technology*, QMC, Inc., July 1993. An approximate expression for the time delay, τ, as it relates to the transmission of a signal between transistors on an integrated circuit is given below.

$$\tau=RC[1+(V_{SAT}/RI_{SAT})]$$

In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path and I_{SAT} and V_{SAT} are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, ρ, of the conductor material. The path capacitance is proportional to the relative dielectric permittivity, K_e, of the dielectric material. A small value of τ requires that the interconnect line carry a current density sufficiently large to make the ratio V_{SAT}/RI_{SAT} small. It follows therefore, that a low-ρ conductor which can carry a high current density and a low-K_e dielectric must be utilized in the manufacture of high-performance integrated circuits.

To meet the foregoing criterion, copper interconnect lines within a low-K_e dielectric will likely replace aluminum-alloy lines within a silicon oxide dielectric as the most preferred interconnect structure. See "Copper Goes Mainstream: Low-k to Follow", *Semiconductor International*, November 1997, pp. 67–70. Resistivities of copper films are in the range of 1.7 to 2.0 $\mu\Omega$cm.; resistivities of aluminum-alloy films are in the range of 3.0 to 3.5 $\mu\Omega$cm.

Despite the advantageous properties of copper, it has not been as widely used as an interconnect material as one would expect. This is due, at least in part, to the difficulty of depositing copper metallization and, further, due to the need for the presence of barrier layer materials. The need for a barrier layer arises from the tendency of copper to diffuse into silicon junctions and alter the electrical characteristics of the semiconductor devices formed in the substrate. Barrier layers made of, for example, titanium nitride, tantalum nitride, etc., must be laid over the silicon junctions and any intervening layers prior to depositing a layer of copper to prevent such diffusion.

A number of processes for applying copper metallization to semiconductor workpieces have been developed in recent years. One such process is chemical vapor deposition (CVD), in which a thin copper film is formed on the surface of the barrier layer by thermal decomposition and/or reaction of gas phase copper compositions. A CVD process can result in conformal copper coverage over a variety of topological profiles, but such processes are expensive when used to implement an entire metallization layer.

Another known technique, physical vapor deposition (PVD), can readily deposit copper on the barrier layer with relatively good adhesion when compared to CVD processes. One disadvantage of PVD processes, however, is that they result in poor (non-conformal) step coverage when used to fill microstructures, such as vias and trenches, disposed in the surface of the semiconductor workpiece. For example, such non-conformal coverage results in less copper deposition at the bottom and especially on the sidewalls of trenches in the semiconductor devices.

Inadequate deposition of a PVD copper layer into a trench to form an interconnect line in the plane of a metallization

layer is illustrated in FIG. 1. As illustrated, the upper portion of the trench is effectively "pinched off" before an adequate amount of copper has been deposited within the lower portions of the trench. This result in an open void region that seriously impacts the ability of the metallization line to carry the electrical signals for which it was designed.

Electrochemical deposition of copper has been found to provide the most cost-effective manner in which to deposit a copper metallization layer. In addition to being economically viable, such deposition techniques provide substantially conformal copper films that are mechanically and electrically suitable for interconnect structures. These techniques, however, are generally only suitable for applying copper to an electrically conductive layer. As such, an underlying conductive seed layer is generally applied to the workpiece before it is subject to an electrochemical deposition process. Techniques for electrodeposition of copper on a barrier layer material have not heretofore been commercially viable.

The present inventors have recognized that there exists a need to provide copper metallization processing techniques that 1) provide conformal copper coverage with adequate adhesion to the barrier layer, 2) provide adequate deposition speeds, and 3) are commercially viable. These needs are met by the apparatus and processes of the present invention as described below.

BRIEF SUMMARY OF THE INVENTION

This invention employs a novel approach to the copper metallization of a workpiece, such as a semiconductor workpiece. In accordance with the invention, an alkaline electrolytic copper bath is used to electroplate copper onto a seed layer, electroplate copper directly onto a barrier layer material, or enhance an ultra-thin copper seed layer which has been deposited on the barrier layer using a deposition process such as PVD. The resulting copper layer provides an excellent conformal copper coating that fills trenches, vias, and other microstructures in the workpiece. When used for seed layer enhancement, the resulting copper seed layer provide an excellent conformal copper coating that allows the microstructures to be filled with a copper layer having good uniformity using electrochemical deposition techniques. Further, copper layers that are electroplated in the disclosed manner exhibit low sheet resistance and are readily annealed at low temperatures.

The disclosed process, as noted above, is applicable to a wide range of steps used in the manufacture of a metallization layer in a workpiece. The workpiece may, for example, be a semiconductor workpiece that is processed to form integrated circuits or other microelectronic components. Without limitation as to the applicability of the disclosed invention, a process for enhancing a seed layer is described.

A process for applying a metallization interconnect structure to a workpiece having a barrier layer deposited on a surface thereof is also set forth. The process includes the forming of an ultra-thin metal seed layer on the barrier layer. The ultra-thin seed layer has a thickness of less than or equal to about 500 Angstroms and may be formed from any material that can serve as a seed layer for subsequent metal deposition. Such metals include, for example, copper, copper alloys, aluminum, aluminum alloys, nickel, nickel alloys, etc. The ultra-thin seed layer is then enhanced by depositing additional metal thereon in a separate deposition step to provide an enhanced seed layer that is suitable for use in a primary metal deposition. The enhanced seed layer has a thickness at all points on sidewalls of substantially all recessed features distributed within the workpiece that is equal to or greater than about 10% of the nominal seed layer thickness over an exteriorly disposed surface of the workpiece.

In accordance with a specific embodiment of the process, a copper-containing metallization interconnect structure is formed. To this end, the ultra-thin seed layer is enhanced by subjecting the semiconductor workpiece to an electrochemical copper deposition process in which an alkaline bath having a complexing agent is employed. The copper complexing agent may be at least one complexing agent selected from a group consisting of EDTA, ED, and a polycarboxylic acid such as citric acid or salts thereof.

Various plating bath compositions suitable for blanket plating, fill-plating of recessed micro-structures, and seed layer enhancement plating are also set forth. A preferred solution for electroplating copper for seed layer enhancement comprises copper sulfate, boric acid, and a complexing agent. The complexing agent is preferably selected from the group consisting of ED, EDTA, and a polycarboxylic acid, such as citric acid. This solution is also suitable for blanket plating and fill-plating of recessed micro-structures.

A plating solution that improves the resistivity of the resulting copper film is also set forth. The plating solution preferably comprises copper sulfate, ammonium sulfate, and ethylene glycol. This solution is also suitable for blanket plating and fill-plating of recessed micro-structures.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. 1 is a cross-sectional view illustrating an interconnect line formed completely by PVD copper.

FIGS. 2A–2E are cross-sectional views through a semiconductor workpiece illustrating the various layers of material as they are applied in accordance with one embodiment of the present invention.

FIG. 3 is a schematic representation of an apparatus suitable for enhancing an ultra-thin seed layer.

FIG. 4A is a graph illustrating the current-potential curves of a plating solution using a polycarboxylic acid, such as citric acid, as a complexing agent.

FIG. 4B a graph illustrating the current-potential curves of a plating solution using EDTA, an amine-containing plating solution, as the complexing agent.

FIG. 4C is a graph of sheet resistance change with annealing temperature for copper films deposited from a bath solution with and without ammonium sulfate.

FIG. 4D is a graph illustrating plating solution conductivity as a function of ethylene glycol concentration in collating solutions with and without ammonium sulfate.

FIG. 5 is a scanning eletromicrograph photograph illustrating an ultra-thin seed layer.

FIG. 6A is a scanning eletromicrograph photograph illustrating an ultra-thin seed layer that has been enhanced in a citric acid bath.

FIG. 6B is a scanning eletromicrograph photograph illustrating an ultra-thin seed layer that has been enhanced in an EDTA bath.

FIG. 7 is a schematic representation of a section of a semiconductor manufacturing line suitable for implementing the disclosed seed layer enhancement steps.

DETAILED DESCRIPTION OF THE INVENTION

This invention employs a novel approach to applying copper metallization to a workpiece, such as a semiconduc-

tor workpiece. In accordance with the invention, an alkaline electrolytic copper bath is used to electroplate copper onto a seed layer, electroplate copper directly onto a barrier layer material, or enhance an ultra-thin copper seed layer which has been deposited on the barrier layer using a deposition process such as PVD. Additionally, a method for applying a metallization layer will be disclosed. Although the disclosed method may be used in connection with a substantial number of different metal compositions, the specific embodiment disclosed herein is directed to the application of a copper-containing metallization layer. To this end, an alkaline electrolytic copper bath is used to enhance an ultra-thin copper seed layer which has been deposited on a barrier layer using a deposition process such as PVD. The enhanced copper seed layer provides an excellent conformal copper coating that allows trenches and vias to be subsequently filled with a copper layer having good uniformity using electrochemical deposition techniques.

A cross-sectional view of a micro-structure, such as trench **5**, that is to be filled with copper metallization is illustrated in FIG. **2**A and will be used to to describe the seed layer enhancement aspects of the present invention. As shown, a thin barrier layer **10** of, for example, titanium nitride or tantalum nitride is deposited over the surface of a semiconductor device or, as illustrated in FIG. **2**A, over a layer of a dielectric **8**, such as silicon dioxide. The barrier layer **10** acts to prevent the migration of copper to any semiconductor device formed in the substrate. Any of the various known techniques, such as CVD or PVD, can be used to deposit the barrier layer depending on the particular barrier material being used. Preferably, the thickness for the barrier layer is approximately 100 to 300 Angstroms.

After the deposition of the barrier layer, an ultra-thin copper seed layer **15** is deposited on the barrier layer **10**. The resulting structure is illustrated in FIG. **2**B. Preferably, the copper seed layer **15** is formed using a vapor deposition technique, such as CVD or PVD. In order to have adequate adhesion and copper coverage, a relatively thick (1000 Angstroms) copper seed layer is usually required. Such a thick seed layer leads to problems with close-off of small geometry trenches, however, when a PVD deposition process is employed for applying the seed layer.

Contrary to traditional thoughts regarding seed layer application, the copper seed layer **15** of the illustrated embodiment is ultra-thin, having a thickness of about 50 to about 500 Angstroms, preferably about 100 to about 250 Angstroms, and most preferably about 200 Angstroms. The ultra-thin copper seed layer can be deposited using a CVD or a PVD process, or a combination of both. PVD is the preferred application process, however, because it can readily deposit copper on the barrier layer **10** with relatively good adhesion. By depositing an ultra-thin seed layer of copper, rather than the relatively thick seed layer used in the prior art, pinching off of the trenches can be avoided.

The use of an ultra-thin seed layer **15** generally introduces its own set of problems. One of the most significant of these problems is the fact that such ultra-thin layers do not generally coat the barrier layer **10** in a uniform manner. Rather, voids or non-continuous seed layer regions on the sidewalls, such as at **20**, are often present in an ultra-thin seed layer **15** thereby resulting in the inability to properly apply a subsequent electrochemically deposited copper layer in the regions **20**. Further, ultra-thin seed layers tend to include spikes, such as at **21**, that impact the uniformity of the subsequent electrolytically deposited metal layer. Such spikes **21** result in high potential regions at which the copper deposits at a higher rate than at other, more level regions. As such, the seed layer **15** is not fully suitable for the traditional electroplating techniques typically used after application of a seed layer.

The present inventors have found that an ultra-thin seed layer can be employed if it is combined with a subsequent electrochemical seed layer enhancement technique. To this end, the semiconductor workpiece is subject to a subsequent process step in which a further amount of copper **18** is applied to the ultra-thin seed layer to thereby enhance the seed layer. A seed layer enhanced by the additional deposition of copper is illustrated in FIG. **2**C. As shown in FIG. **2**C, the void or non-continuous regions **20** of FIG. **2**B have been filled thereby leaving substantially all of the barrier layer **10** covered with copper.

Preferably, the seed layer enhancement process continues until a sidewall step coverage, i.e., the ratio of the seed layer thickness at the bottom sidewall regions **22** to the nominal thickness of the seed layer at the exteriorly disposed side **23** of the workpiece, achieves a value of at least 10%. More preferably, the sidewall step coverage is at least about 20%. Such sidewall step coverage values are present in substantially all of the recessed structures of the semiconductor workpiece. It will be recognized, however, that certain recessed structures distributed within the semiconductor workpiece may not reach these sidewall step coverage values. For example, such structures disposed at the peripheral edges of a semiconductor wafer may not reach these step coverage values. Similarly, defects or contaminants at the situs of certain recessed structures may prevent them from reaching the desired coverage values. The nominal thickness of the enhanced seed layer at the exteriorly disposed side of the workpiece is preferably in the range of 500 angstroms 1600 angstroms.

Although the embodiment of the process disclosed herein is described in connection with copper metallization, it is understood that the basic principle of the enhancement of an ultra-thin seed layer prior to the bulk deposition thereof can be applied to other metals or alloys that are capable of being electroplated. Such metals include iron, nickel, cobalt, zinc, copper-zinc, nickel-iron, cobalt-iron, etc.

A schematic representation of an apparatus **25** suitable for enhancing the ultra-thin copper seed layer is illustrated in FIG. **3**. It will be recognized that this apparatus is also suitable for applying a blanket plating layer and/or full-fill plating of recessed micro-structures As shown, a semiconductor workpiece, such as a semiconductor wafer **30**, is positioned face down in a bath **35** of electroplating solution. One or more contacts **40** are provided to connect the wafer **30** to a plating power supply **45** as a cathode of an electroplating cell. An anode **50** is disposed in the bath **35** and is connected to the plating power supply **45**. Preferably, a diffuser **55** is disposed between the anode **50** and the wafer/cathode **30**. The wafer **30** may be rotated about axis **60** during the enhancement process. Anode **50** may be provided with a dielectric shield **65** at a backside thereof which faces an incoming stream of plating bath fluid.

As noted above, certain aspects of the present invention relate to new and useful plating solutions. These solutions can be used for blanket plating, full-fill of the recessed micro-structures, seed layer enhancement, etc. The preferred electrolytic bath solution for enhancing the seed layer is an alkaline copper bath in which copper ions are complexed with a complexing agent. A preferred composition and range of concentrations for the various components of the plating bath include the following:

1. Copper sulfate: 0.03M to 0.25M (preferably, 0.04);
2. Complexing agent: complex to metal ratios from 1 to 4, preferably 2;
3. Boric acid: 0.01M to 0.5M, preferably 0.05M; and
4. pH: 5–13, preferably 9.5.

A preferred source of copper ions is copper sulfate ($CuSO_4$). The concentration of copper sulfate in the bath is preferably within the range of 0.03 to 0.25 M, and is more preferably about 0.1 M.

Complexing agents that are suitable for use in the present invention form a stable complex with copper ions and prevent the precipitation of copper hydroxide. Ethylene diamine tetracetic acid (EDTA), ethylene diamine (ED), citric acid, and their salts have been found to be particularly suitable copper complexing agents. The molar ratio of complexing agent to copper sulfate in the bath is preferably within the range of 1 to 4, and is preferably about 2. Such complexing agents can be used alone, in combination with one another, or in combination with one or more further complexing agents.

The electrolytic bath is preferably maintained at a pH of at least 9.0. Potassium hydroxide, ammonium hydroxide, tetramethylammonium hydroxide, or sodium hydroxide is utilized to adjust and maintain the pH at the desired level of 9.0 or above. A preferred pH for a citric acid or ED bath is about 9.5, while a preferred pH for an EDTA bath is about 12.5. As noted above, the complexing agent assists in preventing the copper from precipitating at the high pH level.

Additional components can be added to the alkaline copper bath. For example, boric acid (H_3BO_3) aids in maintaining the pH at 9.5 when citric acid or ED is used as the complexing agent, and provides brighter copper deposits when added to an electrolytic bath containing EDTA as the complexing agent. If boric acid is added, its concentration in the bath is preferably within the range of 0.01 to 0.5 M.

In general, the temperature of the bath can be within the range of 20 to 35° C., with 25° C. being a preferred temperature. The current densily for electrolytically depositing copper to enhance the copper seed layer can be 1 to 5 milliamps/cm^2, while a plating time of about 1 to about 5 minutes is sufficient to enhance the copper seed layer. The plating waveform may be, for example, a forward periodic pulse having a period of 2 msec at a 50% duty cycle.

An amine free acid complexing agent, for example, a polycarboxylic acid, such as citric acid, and salts thereof, is preferable to the use of EDTA or ED. EDTA and ED include amine groups. These amine groups often remain on the surface of the semiconductor workpiece after rinsing and drying of the wafer. Subsequent processes, particularly such processes as photolithographic processes, may be corrupted by the reactions resulting from the presence of these amine groups. The amine groups may, for example, interfere with the chemical reactions associated with the exposing and/or curing of photoresist materials. As such, amine free complexing agents are particularly suitable in processes in which a photolithographic process follows an electrodeposition process.

A further advantage of using a polycarboxylic acid, such as citric acid, stems from the fact that the magnitude of the voltage potential at which the copper is plated is greater than the magnitude of the voltage potential at which the copper is plated in a bath containing EDTA. This is illustrated in FIGS. 4A and 4B where FIG. 4A is a current-potential graph for a citric acid bath, and FIG. 4B is a current-potential graph for an EDTA bath. Electroplating takes place at the voltage where the corresponding current increases abruptly. This plating voltage is referred to as the deposition potential, which is approximately −1.25 volts as shown in FIG. 4A for a bath employing citric acid as the complexing agent, and is approximately −1.0 volts as shown in FIG. 4B for a bath employing EDTA as the complexing agent. The current peaks (**70** **70'** for the a bath containing a citric acid, and **72**, **72'** for the bath containing the EDTA) are the limiting currents which are mainly determined by mass transfer and the concentration of copper ions in the plating solutions. As illustrated, the magnitude of the current and the particular plating potential is slightly dependent on the substrate material. The different substrate results are illustrated in FIGS. 4A and 4B, where **70** and **72** are the curves for a copper substrate material, and **70'** and **72'** are curves for a copper substrate material comprised of copper with a copper oxide coating. It is noted that additional peaks occur on oxidized copper in the same electrolytes. These peaks are related to the electrochemical reduction of copper oxide to metallic copper before the alkaline electrochemical copper deposition.

It is believed that a copper layer plated at a higher plating potential in an alkaline bath provides greater adhesion to the underlying barrier layer than a copper layer plated at a lower plating potential in an acid bath. For copper to adhere to the barrier material, it is thought that copper ions must impinge on the barrier surface with sufficient energy to penetrate a thin oxidized or contaminated layer at the barrier surface. It is therefore believed that a copper layer deposited at a higher magnitude plating potential adhere is better to the exposed barrier layer during the plating process when compared to a layer plated using a smaller magnitude plating potential. This factor, combined with the inter-copper chemical bond between the PVD copper and the electrochemically deposited copper provides for an enhanced seed layer having excellent electrical as well as barrier adhesion properties. Such characteristics are also desirable for films used in blanket plating, full-fill plating, pattern plating, etc.

It has been found that the resistivity of the deposited copper film is directly related to the resistivity of the plating bath solution. Additives that assist in lowering the resistivity of the solution therefore provide a corresponding reduction in the resistivity of the deposited film.

Experimental results indicate that addition of ammonium sulfate significantly reduces the resistivity of the plating bath solution and, as such, the deposited film. The sheet resistance obtained for different amounts of ammonium sulfate are compared in the graph FIG. 4C. As can be seen, the highest sheet resistance, either with or without annealing at high temperatures, was obtained in the bath containing no ammonium sulfate. If ammonium hydroxide was used to adjust pH in which a trace amount of ammonium sulfate is introduced to the bath, the sheet resistance was reduced from 76 to 23. As the concentration of ammonium sulfate increased from 0.1 M to 0.5 M, the sheet resistance continuously decreased in a corresponding manner.

Although ammonium sulfate assists in reducing the sheet resistance of the deposited copper layer, experimental results indicate that it reduces the conformability of the resulting copper film. However, the addition of ethylene glycol to the ammonium sulfate containing solution substantially increases the conformability of the resulting deposit. FIG. 4D illustrates the relationship between the concentration of ethylene glycol and the conductivity of a plating solution containing 0.2M the of ammonium sulfate.

A preferred composition and range of concentrations for the various components of a plating bath having ammonium sulfate include the following:

1. Copper sulfate: 0.03M to 0.5M (preferably, 0.25M);
2. Complexing agent: complex to metal ratios from 1 to 4, preferably 2 using ED;
3. Ammonium sulfate: 0.01M to 0.5M, preferably 0.3M; and
4. Boric acid: 0.00 to 0.5M, preferably 0.2M.

As noted above, such a bath composition can be used for blanket plating, pattern plating, full-fill plating, and seed layer enhancement.

With reference again to the specific seed layer enhanced aspects of the present invention, the enhanced seed layer of FIG. 2C is suitable for subsequent electrochemical copper deposition. This subsequent copper deposition may take place in an alkaline bath within the apparatus employed to enhance the seed layer. This may be followed by a low-temperature annealing process that assists in lowering the resistivity of the deposited copper. Such a low-temperature annealing process preferably takes place at a temperature below about the 250 degrees Celsius and, more preferably, below about 100 degrees Celsius. When a low-K dielectric material is employed to isolate the copper structures, the upper annealing temperature limit should be chosen to be below the degradation temperature of the dielectric material.

Although the foregoing alkaline bath compositions may be used for the entire electrochemical deposition process, subsequent copper deposition may take place in an acid environment where plating rates are substantially higher than corresponding rates associated with alkaline plating baths. To this end, the semiconductor workpiece is preferably transferred to an apparatus wherein the workpiece is thoroughly rinsed with deionized water and then transferred to an apparatus similar to that of FIG. 3 wherein the plating bath is acidic. For example, one suitable copper bath comprises 170 g/l H_2SO_4, 17 g/l copper and 70 ppm Chloride ions with organic additives. The organic additives are not absolutely necessary to the plating reaction. Rather, the organic additives may be used to produce desired film characteristics and provide better filling of the recessed structures on the wafer surface. The organic additives may include levelers, brighteners, wetting agents and ductility enhancers. It is during this deposition process that the trench **5** is substantially filled with a further layer of electrochemically deposited copper **22**. The resulting filled cross-section is illustrated in FIG. 2D. After being filled in this manner, the barrier layer and the copper layers disposed above the trench are removed using any suitable process thereby leaving only the trench **5** with the copper metallization and associated barrier material as shown in FIG. 2E.

Use of an alkaline electrolytic bath to enhance the copper seed layer has particular advantages over utilizing acid copper baths without seed layer enhancement. After deposition of the PVD copper seed layer, the copper seed layer is typically exposed to an oxygen-containing environment. Oxygen readily converts metallic copper to copper oxide. If an acid copper bath is used to plate copper onto the seed layer after exposure of the seed layer to an oxygen containing environment, the acid copper bath would dissolve copper oxide that had formed, resulting in voids in the seed layer and poor uniformity of the copper layer deposited on the seed layer. Use of an alkaline copper bath in accordance with the disclosed embodiment avoids the problem by advantageously reducing any copper oxide at the surface of the seed layer to metallic copper. Another advantage of the alkaline copper bath is that the plated copper has much better adhesion to the barrier layer than that plated from an acid copper bath. Additional advantages of the seed layer enhancement aspects of the present invention can be seen from the following Example.

EXAMPLE 1

Comparison of Acid Copper Plating With and Without Seed Layer Enhancement

Semiconductor wafers **1**, **2** and **3** were each coated with a 200 Angstrom PVD copper seed layer. In accordance with the present invention, wafers **1** and **2** had seed layer enhancement from citric acid and EDTA baths, respectively, the compositions of which are set forth below:

Bath for Wafer 1: 0.1 M Cu SO_4+0.2 M Citric acid+0.05 M H_3BO_3 in D.I. water at pH 9.5, temperature 25° C.

Bath for Wafer 2: 0.1 M Cu SO_4+0.2 M EDTA acid+0.05 H_3BO_3 in D.I. water at pH 12.5, temperature 25° C.

Wafer **3** did not have any seed layer enhancement.

The three wafers were then plated with a 1.5 micron copper layer from an acid copper bath under identical conditions. The following Table compares the uniformities, as deduced from sheet resistance measurements, of the three wafers after the deposition of a copper layer having a nominal thickness of 1.5 microns.

TABLE 1

Wafer	Enhancement Bath	Current Density	Non-uniformity Standard deviation (%, 1σ)
1	Citrate	3 min. at 2 mA/cm^2	7.321
2	EDTA	3 min. at 2 mA/cm^2	6.233
3	None	0	46.10

As can be seen from the results in Table 1 above, seed layer enhancement in accordance with the disclosed process provides excellent uniformity (6 to 7%) compared to that without seed layer enhancement (46%). This is consistent with observations during visual examination of the wafer after 1.5 micron electroplated copper had been deposited. Such visual examination of the wafer revealed the presence of defects at wafer electrode contact points on the wafer without seed layer enhancement.

FIGS. **5**, **6A** and **6B** are photographs taken using a SEM. In FIG. **5**, an ultra-thin seed layer has been deposited on the surface of a semiconductor wafer, including micro-structures, such as trenches **85**. As shown, void regions are present at the lower comers of the trenches. In FIG. **6A**, the seed layer has been enhanced in the manner described above in a bath containing citric acid as the complexing agent. This enhancement resulted in a conformal copper seed layer that is very suited for subsequent electrochemical deposition of copper metallization.

FIG. **6B** illustrates a seed layer that has been enhanced in a bath containing EDTA as the complexing agent. The resulting seed layer includes larger grain sizes that project as spikes from the sidewalls of the trenches. These sidewall grain projections make subsequent electrochemical deposition filling of the trenches more difficult since they localize a higher plating rate resulting in non-uniformity of the subsequent electrochemical deposition. This effect is particularly noticeable in recessed micro-structures having small dimensions. As such, a complexing agent such as citric acid is more preferable when filling small micro-structures. Results comparable for copper baths containing citric acid have also been achieved using ED as the complexing agent.

FIG. **7** is a schematic representation of a section of a semiconductor manufacturing line **90** suitable for implementing the foregoing processes. The line **90** includes a

vapor deposition tool or tool set **95** and an electrochemical copper deposition tool or tool set **100**. Transfer of wafers between the tools/tool sets **95** and **100** may be implemented manually or through an automated transfer mechanism **105**. Preferably, automated transfer mechanism **105** transfers workpieces in a pod or similar environment. Alternatively, the transfer mechanism **105** may transfer wafers individually or in an open carrier through a clean atmosphere joining the tools/tool sets.

In operation, vapor deposition tool/tool set **95** is utilized to apply an ultra-thin copper seed layer over at least portions of semiconductor workpieces that are processed on line **90**. Preferably, this is done using a PVD application process. Workpieces with the ultra-thin seed layer are then transferred to tool/tool set **100**, either individually or in batches, where they are subject to electrochemical seed layer enhancement at, for example, processing station **10**. Processing station **10** may be constructed in the manner set forth in FIG. **3**. After enhancement is completed, the workpieces are subject to a full electrochemical deposition process in which copper metallization is applied to the workpiece to a desired interconnect metallization thickness. This latter process may take place at station **110**, but preferably occurs at further processing station **115** which deposits the copper metallization in the presence of an acidic plating bath. Before transfer to station **115**, the workpiece is preferably rinsed in DI water at station **112**. Transfer of the wafers between stations **110**, **112**, and **115** may be automated by a wafer conveying system **120**. The electrochemical deposition tool set **100** may be implemented using, for example, an LT-210™ model or an Equinox™ model plating tool available from Semitool, Inc., of Kalispell, MT.

Numerous modifications may be made to the foregoing system without departing from the basic teachings thereof. Although the present invention has been described in substantial detail with reference to one or more specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the scope and spirit of the invention as set forth in the appended claims.

What is claimed is:

1. A process for applying a metal structure to a workpiece comprising:

providing a first electroplating bath including copper sulfate as a source of metal ions as a principal metal species to be deposited during subsequent electroplating, ammonium sulfate, a complexing agent, and ethylene glycol;

providing a workpiece on which one or more microelectronic devices are to be formed;

exposing at least one surface of the workpiece to the first electroplating bath;

providing electroplating power between the at least one surface of the workpiece and an anode disposed in electrical contact with the first electroplating bath to electroplate copper onto the at least one surface of the workpiece in an electrolytic first deposition process; and

depositing additional copper onto the copper deposited in the first deposition process using a second deposition process that is different than the first electrolytic deposition process.

2. The process of claim **1**, wherein the copper sulfate is included at a level of 0.03 to 0.25 M.

3. The process of claim **1**, wherein the first electroplating bath comprises an alkaline bath.

4. The process of claim **3**, wherein the alkaline bath has a pH of at least 9.0.

5. The process of claim **3**, wherein the alkaline bath is pH adjusted with an alkaline agent selected from the group consisting of potassium hydroxide, ammonium hydroxide, tetramethylammonium hydroxide and sodium hydroxide.

6. The process of claim **1**, wherein the second deposition process occurs in an acidic electrolytic bath.

7. The process of claim **1**, wherein metal is deposited in the second deposition process at a higher rate than in the first deposition process.

8. The process of claim **1**, wherein the ammonium sulfate is included at a level of 0.1 to 0.5 M.

9. The process of claim **1**, further comprising depositing a barrier layer on the surface of the workpiece before the first deposition process.

10. The process of claim **9**, wherein metal is plated directly onto the barrier layer in the first deposition process.

11. The process of claim **9**, further comprising depositing an ultra-thin seed layer of metal onto the barrier layer before the first deposition process.

12. The process of claim **1**, wherein the complexing agent is selected from the group consisting of ED, EDTA, and a polycarboxylic acid.

13. The process of claim **12**, wherein the complexing agent is citric acid.

14. A process for applying a metal structure to a workpiece comprising:

providing a first electroplating bath including copper sulfate as a source of metal ions as a principal metal species to be deposited during subsequent electroplating, a complexing agent, and ethylene glycol;

providing a workpiece on which one or more microelectronic devices are to be formed,

exposing at least one surface of the workpiece to the first electroplating bath;

providing electroplating power between the at least one surface of the workpiece and an anode disposed in electrical contact with the first electroplating bath to electroplate copper onto the at least one surface of the workpiece in an electrolytic first deposition process at a first deposition rate; and

depositing additional copper onto the copper deposited in the first deposition process using a second deposition process at a second deposition rate that is higher than the first deposition rate.

15. A process for applying a metal structure to a workpiece comprising:

providing a workpiece on which one or more microelectronic devices are to be formed;

depositing a barrier layer on at least one surface of a workpiece;

providing a first electroplating bath including copper sulfate as a source of principal metal species to be deposited during subsequent electroplating, ethylene glycol, a metal ion complexing agent, and an alkaline agent in an amount to adjust the pH of the first electroplating bath to a pH of at least 9.0;

exposing the least one surface of the workpiece including the barrier layer to the first electroplating bath;

providing electroplating power between the at least one surface of the workpiece and an anode disposed in electrical contact with the first electroplating bath to electroplate copper directly onto the barrier layer of the workpiece in an electrolytic first deposition process; and

depositing additional copper onto the copper deposited in the first deposition process using a second deposition process at a second deposition rate that is higher than a rate at which copper is deposited in the first deposition process.

16. The process of claim 15, wherein the alkaline agent selected from the group consisting of potassium hydroxide, ammonium hydroxide, tetramethylammonium hydroxide and sodium hydroxide.

17. The process of claim 15, wherein the second deposition process occurs in an acidic electrolytic bath.

18. The process of claim 15, wherein the complexing agent is selected from the group consisting of ED, EDTA, and a polycarboxylic acid.

19. The process of claim 18, wherein the complexing agent is citric acid.

20. A process for applying a metal structure to a workpiece comprising:

providing a first electroplating bath including copper sulfate as a source of metal ions as a principal metal species to be deposited during subsequent electroplating, a complexing agent, ethylene glycol, and an alkaline agent in an amount sufficient to raise the pH of the bath to at least 9.0;

providing a workpiece on which one or more microelectronic devices are to be formed;

exposing at least one surface of the workpiece to the first electroplating bath;

providing electroplating power between the at least one surface of the workpiece and an anode disposed in electrical contact with the first electroplating bath to electroplate copper onto the at least one surface of the workpiece in an electrolytic first deposition process; and

depositing additional copper onto the copper deposited in the first deposition process using a second deposition process that is different than the first electrolytic deposition process.

21. A copper electroplating solution comprising copper sulfate as a source of copper ions at a level so as to be the principal metal species, ammonium sulfate, and ethylene glycol at a levl of greater than 0 to 1.0 Molar, the solution being formulated so as to be suitable for electrodeposition of copper onto a microelectronic workpiece.

22. The solution of claim 21, further comprising a complexing agent.

23. The solution of claim 22 wherein the complexing agent is selected from the group consisting of ED, EDTA, and a polycarboxylic acid.

24. The solution of claim 23 wherein the complexing agent is citric acid.

25. The solution of claim 21, further comprising an alkaline agent in an amount sufficient to increase the pH of the solution to at least 9.0.

26. The solution of claim 21, wherein the ammonium sulfate is included at the level of 0.1 to 0.5 M.

27. The solution of claim 21, further comprising boric acid at a level of 0.01 Molar to 0.5 Molar.

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(12) **United States Patent**
Gross et al.

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(45) **Date of Patent: Oct. 2, 2001**

(54) **PROCESS FOR SEMICONDUCTOR DEVICE FABRICATION HAVING COPPER INTERCONNECTS**

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(57) **ABSTRACT**

A process for fabricating a semiconductor device with copper interconnects is disclosed. In the process of the present invention, a layer of dielectric material is formed on a substrate. At least one recess is formed in the layer of dielectric material. Barrier layers and seed layers for electroplating are then deposited over the entire surface of the substrate. The recess is then filled with copper by electroplating copper over the surface of the substrate. The electroplated copper has an average grain size of about 0.1 μm to about 0.2 μm immediately after deposition. The substrate is then annealed to increase the grain size of the copper and to provide a grain structure that is stable over time at ambient conditions and during subsequent processing. After annealing, the average grain size of the copper is at least about 1 μm in at least one dimension. The copper that is electroplated on the dielectric layer is then removed using an expedient such as chemical mechanical polishing. The copper that remains is the copper in the recess.

9 Claims, 1 Drawing Sheet

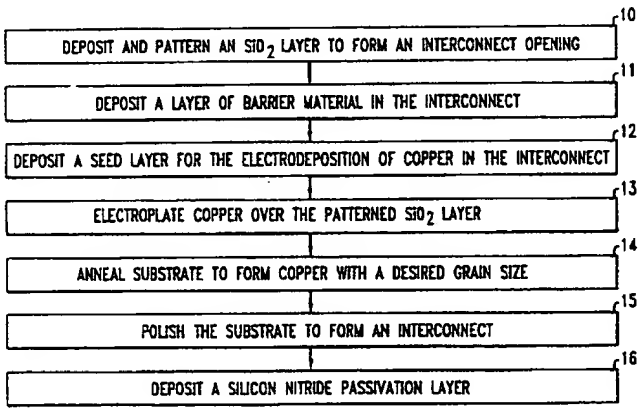
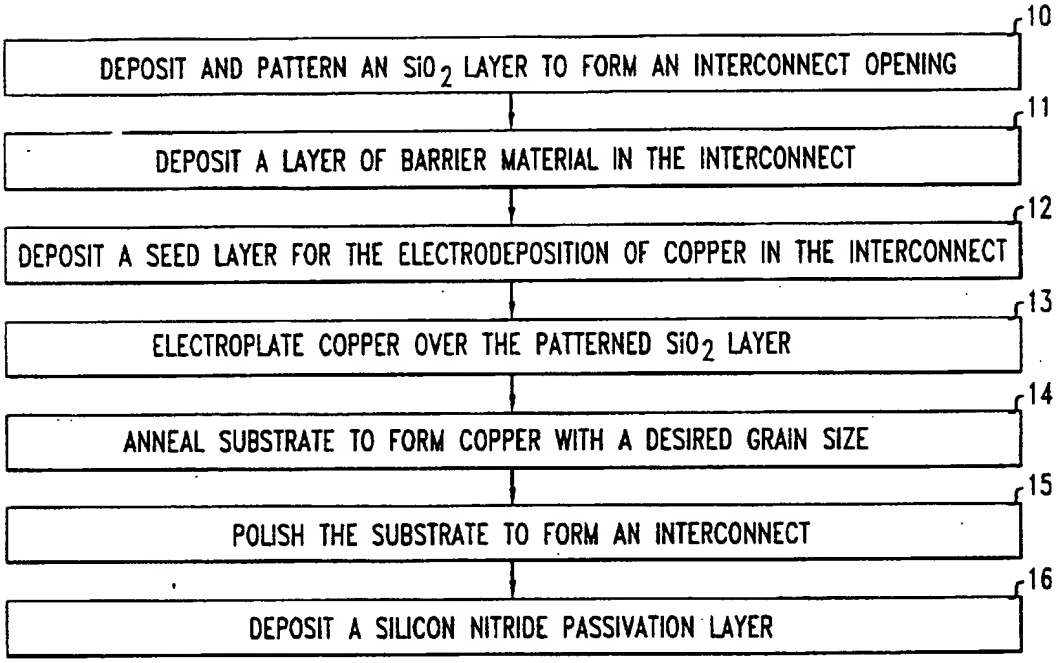


FIG. 1


10
DEPOSIT AND PATTERN AN SiO_2 LAYER TO FORM AN INTERCONNECT OPENING
11
DEPOSIT A LAYER OF BARRIER MATERIAL IN THE INTERCONNECT
12
DEPOSIT A SEED LAYER FOR THE ELECTRODEPOSITION OF COPPER IN THE INTERCONNECT
13
ELECTROPLATE COPPER OVER THE PATTERNED SiO_2 LAYER
14
ANNEAL SUBSTRATE TO FORM COPPER WITH A DESIRED GRAIN SIZE
15
POLISH THE SUBSTRATE TO FORM AN INTERCONNECT
16
DEPOSIT A SILICON NITRIDE PASSIVATION LAYER

PROCESS FOR SEMICONDUCTOR DEVICE FABRICATION HAVING COPPER INTERCONNECTS

BACKGROUND OF THE INVENTION

1. Technical Field

This invention is directed to a process for fabricating integrated circuit devices and, in particular, to semiconductor devices that have copper interconnects.

2. Art Background

As devices are scaled to sub-micron dimensions, formation of reliable sub-micron interconnection (interconnects) becomes increasingly difficult. Many techniques have been used to form interconnects. However, as the dimensions of sub-micron interconnects get smaller, current techniques are becoming less useful.

For example, techniques that require the interconnects to be formed by patterning a layer of metal using lithographic techniques, in which the pattern defined in a layer of energy sensitive material is transferred into the underlying metal layer by etch expedient, have several problems. In these techniques, contact holes (windows or vias) are formed in a layer of a dielectric material. The contact holes are then filled with metal by depositing a metal layer over the dielectric layer. The portion of the deposited metal layer overlying the dielectric layer is then removed using an expedient such as etching or chemical mechanical polishing (CMP). The portion of the metal layer that remains is the portion in the contact holes formed in the dielectric layer.

A second layer of metal is then formed over the dielectric layer with the metal-filled contact holes. The second metal layer is patterned to form the interconnect wires in the conventional subtractive process. Typically the metal filling the contact holes is one metal (e.g., CVD (chemical vapor deposited) tungsten) and the patterned metal is a second metal (e.g., aluminum). The second metal layer is patterned using lithographic techniques.

Such a process has certain problems associated therewith. Specifically, the patterned aluminum layer is subject to sidewall corrosion. Also, the spaces between the patterned metal lines must be subsequently filled with a dielectric layer before further processing. Furthermore, the use of dissimilar metals for the interconnects (e.g., tungsten) and the wires (e.g., aluminum) adversely affects both the mechanical strength and the electrical quality of the interconnect.

Copper is currently under investigation as an interconnect material because it has a low cost and a low resistivity. However, it is difficult to etch copper. Therefore processes that require the metal interconnect to be etched are not useful for forming copper interconnects. A promising technique for forming interconnects is a dual damascene process (or a combination of two single damascene processes). In a dual damascene process a single dielectric layer is deposited and patterned using a two-step etch process. The first step etches contact openings through half or more of the dielectric layer thickness and the second etch step etches the contact openings through the remaining dielectric thickness to the underlying layer and also the interconnect channels (i.e., trenches) part way through the dielectric layer.

The dual damascene process is advantageous for copper interconnect formation compared to the conventional subtractive process because in dual damascene, lithographic techniques and etching expedients are not required to pattern a layer of copper. However, in dual damascene, copper deposition is complicated because the contact openings may have an aspect ratio (i.e. the ratio of the height to the width of the recess) of 2:1, 3:1, or more. The high aspect ratio makes sputter deposition difficult. Copper may be deposited by CVD within the contact openings and interconnect channels. However, copper is difficult and/or expensive to deposit by CVD. As a result, copper is not typically deposited by CVD in production.

Electroless metal deposition (i.e., electroless plating) has been investigated as a technique for depositing copper onto a patterned layer of dielectric material. In this technique the surfaces to be plated (e.g., contact openings (windows or vias) and interconnect channels) must be pretreated before the metal is deposited in order to effect electroless deposition. Low deposition rates and issues of bath stability make this approach unattractive for use in production. In addition, current surface activation techniques such as physical vapor deposition (PVD, e.g., sputtering) of a catalytic metal or treatment with an activating solution are either difficult or incompatible with current processes for device fabrication.

A major advantage of copper is its relatively low cost and low resistivity. However, it has a relatively large diffusion coefficient into silicon, silicon dioxide, and low dielectric constant polymers such as polyimide. Copper from an interconnect may diffuse through the silicon dioxide or polymer layer and into the underlying silicon. Copper diffusion into the underlying silicon substrate can degrade the transistor characteristics of the resulting device. Copper interconnects should be encapsulated by at least Ione diffusion barrier to prevent diffusion into the silicon dioxide layer. The formation of this diffusion barrier is another problem associated with copper interconnect formation.

As noted in U.S. Pat. No. 5,627,102 to Shinriki et al., one problem associated with the formation of metal interconnects is that voids form in the metal filling the recess. Such faulty fill-up leads to a failure to establish a sound electrical contact. The problem of faulty fill-up increases with increasing aspect ratios. Consequently, as the width of the recess decreases, the problems associated with faulty fill-up increase.

Accordingly, a process for making copper interconnects that addresses the current problems associated with copper interconnect formation is desired.

SUMMARY OF THE INVENTION

The present invention is directed to a process for semiconductor device fabrication in which at least one of the interconnects is made of copper. In the process of the present invention, a copper or copper alloy is electroplated into a recess formed in the surface of a dielectric layer on a semiconductor substrate (i.e., a single damascene process). The dielectric layer may be a material such as silicon dioxide or a low dielectric constant polymer such as, for example, polyimide or polyaryl ethers. For convenience, the recess is referred to as a trench, although one skilled in the art will appreciate that the configuration of the recessed portion is a matter of design choice.

Since copper may diffuse into the dielectric material, a barrier to copper diffusion is typically required. Such a barrier is typically formed on the recess in the dielectric layer before the copper is deposited therein. However, the barrier may also be formed by doping the copper and by outdiffusing the dopant material to form a barrier layer at the interface between the copper and the dielectric, after the copper is deposited in the recess, to prevent copper diffusion into the adjacent dielectric material. Materials that act as a

barrier to copper diffusion are well known to one skilled in the art. Examples of suitable barrier materials include tantalum, tantalum nitride and titanium nitride. The thickness of a barrier layer is at least about 10 nm.

Before electroplating copper in the trench, a seed layer is formed therein. The thickness of the seed layer is at least about 5 nm. The seed layer acts as a cathode for electroplating copper into the recess. The copper seed layer is deposited using a conventional expedient such as PVD, CVD, or electroless plating.

A layer of copper is then electroplated onto the barrier-coated surface of the dielectric layer formed on the substrate. The copper layer is formed over the entire surface of the substrate. The copper layer is then polished back so that the only portion of the copper that remains is the portion of the copper in the trench. The electroplated copper layer is polished back using conventional expedients well known to one skilled in the art. Chemical mechanical polishing is one example of a suitable expedient.

Either before or after the electroplated layer of copper is polished, the substrate is then annealed. The temperature of the anneal, and the duration of the anneal, are selected to bring the grain structure of the electroplated copper from its as-deposited small grain state to a large grain state. For purposes of the present invention, a small grain state is an average grain size of about 0.1 μm to about 0.2 μm. A large grain state is a grain size that is at least one micron in at least one dimension. In certain embodiments, the grain size is constrained by the size of the recess in which the copper is deposited. For example, when the copper is deposited in a trench having a width of less than one micron, the average large grain size is at least as large as the width of the trench into which the copper is deposited and at least about 1 μm in the length direction of the trench. Within the defined range, the smaller the grain size when the copper is deposited, the better the fill. However, after the copper is deposited, it is advantageous to increase the grain size of the copper to the large grain state in order to improve the electrical characteristics of resulting device.

When small grain copper is electroplated using baths with organic additives, the grain structure of the copper is not stable at ambient conditions. In the process of the present invention, the electroplated copper is annealed after deposition in order to provide a copper grain structure that is stable over time.

In the embodiments of the present invention in which the width of the trench is about 0.1 μm to about 5 μm, it is advantageous if the average diameter of the grains in the plated copper film (in the as-deposited small grain state) is about 0.1 μm to about 0.2 μm. In order to obtain large grain state copper with the requisite stability, the substrate is annealed at a temperature in the range of about 100° C. to about 400° C. for about 1 minute to about 1 hour in a non-oxidizing environment. For purposes of the present invention, a non-oxidizing environment is either a vacuum or a non-oxidizing gas such as hydrogen, nitrogen, or argon.

After the copper layer is both polished back and annealed, a passivation layer is formed over the substrate. The passivation layer is intended to prevent the copper interconnect from oxidation and diffusion. One example of a suitable passivation layer material is silicon nitride (Si_3N_4).

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a flow diagram of one embodiment of the present invention.

DETAILED DESCRIPTION

The embodiments of the present invention form an interconnect channel and a copper-containing interconnect within a semiconductor device. In general, a dielectric layer is deposited over a substrate and patterned to form an interconnect channel. An interconnect layer is deposited over the patterned dielectric layer and within the interconnect channel. The substrate is polished with a polishing slurry to remove the portion of the interconnect layer that lies on the patterned dielectric layer, thereby forming the interconnect. Either before or after the interconnect layer is polished, the substrate is annealed. The temperature and duration of the anneal are selected to provide a copper-containing interconnect layer in which the copper has a desired grain size. The interconnect layer may include a barrier layer and a seed layer in addition to the copper layer. If needed, a diffusion barrier layer may be deposited before forming another interconnect level. A passivation layer is deposited over each interconnect level.

The interconnect level is typically formed over a layer of dielectric material with contacts formed therein. The interconnect is in electrical contact with at least one underlying metal feature (window, via) formed in the underlying dielectric layer. In the process of the present invention, the metal features in the underlying layer are also formed by electroplating copper.

A number of materials may be used with the present invention. In general, the dielectric layer is typically either silicon nitride, silicon dioxide doped or undoped), silicon oxynitride, fluoropolymer, polyaryl ether, or polyimide. The interconnect metal is copper.

Since copper has a tendency to diffuse into dielectric materials generally and silicon dioxide in particular, a layer of material that acts as a barrier to diffusion is required. This layer can be formed by either deposition of a barrier layer prior to electroplating copper onto the substrate, or by outdiffusion from the copper itself. If the barrier layer is a separate layer of material, examples include silicon nitride, phosphosilicate glass (PSG), silicon oxynitride, aluminum oxide (Al_xO_y), tantalum, titanium nitride, niobium, or molybdenum. These material are deposited by conventional expedients such as CVD or PVD.

The process of the present invention is used to make copper interconnects to device structures including polysilicon gates, word lines, source regions, drain regions, bit lines, base emitters, collectors, etc. It will be readily apparent to one skilled in the art that the present invention can be used with any semiconductor technology such as, for example, MOS (metal-oxide-semiconductor) devices (e.g., NMOS, PMOS, CMOS, and BiCMOS), bipolar devices, multi-chip modules, and III–V semiconductors.

FIG. 1 includes a flow diagram of one embodiment of the present invention. In step **10**, a silicon dioxide layer is formed on a silicon substrate (the top layer of which is typically a patterned layer of dielectric material with contacts to underlying devices formed therein) and patterned to form an interconnect channel. In step **11** of the described embodiment, a layer that acts as a barrier to the diffusion of copper is deposited over the substrate and into the interconnect channel. In step **12**, a layer of material that functions as a cathode during the subsequent electrodeposition of copper is formed over the patterned dielectric layer and in the interconnect channel.

In step **13**, copper is then electroplated over the patterned dielectric layer and in the interconnect channel. In step **14** the substrate is then annealed to provide copper having a large grain structure with the requisite stability. The substrate is then chemically mechanically polished (**15**) to remove the portion of the copper layers that lies on the

surface of the patterned silicon dioxide layer. In the process of the present invention, the polishing and annealing steps are performed interchangeably. A silicon nitride passivation layer is formed over each interconnect layer in step **16**.

EXAMPLE 1

Damascene trenches were formed in a 0.5 μm thick layer of silicon dioxide formed on a 150 mm silicon wafers. The silicon dioxide layer was formed from PETEOS (plasma enhanced tetraethyl orthosilicate). The trenches were formed using eight different width and space combinations.

Trench widths were in the range of 0.3 μm to 5 μm. These widths represent interconnect widths that might be found from the lower to the upper levels of circuit wiring. The damascene trenches were prepared as grating arrays (i.e., many trenches of equal widths spaced equally apart). For the submicron trench widths (0.3 μm, 0.5 μm, and 0.8 μm) gratings with spacings ranging from roughly equal to the trench width to on the order of 3 μm were made to examine proximity effects.

After the trenches were formed, a 50 nm-thick layer of tantalum nitride was formed on the oxide using PVD. The tantalum nitride was a barrier to the diffusion of copper into the oxide and an adhesion layer. A 100 nm-thick layer of copper was then formed over the layer of tantalum nitride to serve as a cathode for electroplating. The copper film was also formed by PVD. The PVD films were formed sequentially on the wafers, without a vacuum break, by DC magnetron sputtering in a M2i™ cluster deposition tool from Novellus of San Jose, Calif. The tantalum nitride was deposited using 3 kW power (no bias) and a 1:1 collimator. The deposition pressure was 2.9 mTorr and the flow rates of argon and nitrogen were both 35 sccm. The wafer temperature was 150° C. The copper was deposited using 3.1 kW of power (no bias) and a 1:1 collimator. The deposition pressure was standard for PVD copper deposition and the flow rate of argon was 35 sccm. The wafer temperature was 50° C.

The copper was electroplated onto the wafers using an Equinox™ fountain plating system from Semitool of Kalispell, Mont. The wafers were placed in an CUBATH® SC bath that is commercially obtained from Enthone. The bath had a copper sulfate/sulfuric acid plating chemistry. A pulse waveform with a current of 4.9 amp cycled at 95 msec on and 35 msec off was used to electroplate the copper onto the substrate. Copper was plated to a coulometric equivalent of a 1 μm film on an unpatterned 150 mm diameter silicon wafer. The copper films, as plated, were observed to be fine-grained and highly reflective, with a uniform grain size of about 0.1 μm to about 0.2 μm.

Some of the copper-plated substrates were then annealed at 400° C. for one hour in a tube furnace at atmospheric pressure in forming gas (N_2/10% H_2). The grain size of the annealed copper films were compared with the grain size of unannealed copper films. The grain size of the unannealed copper films was observed to increase over time. At room temperature, the grain size of the unannealed copper films increased from an as-deposited average diameter of 0.1 μm to 0.2 μm. Over a period of hours to weeks, the grain size of the unannealed films was observed to increase to greater than 1 μm. The increase in grain size did not occur uniformly. The grain size increase began at isolated points (nucleation sites) in the film and the size of the sites and the number of sites was observed to increase over time. Such change in the copper grain size over a long period of time is not desired because it is uncontrolled and dynamic. The copper film had a mixture of large and small grains for a long period of time.

By contrast, the annealed copper had a uniformly large grain size structure. There was no mixture of large and small grains. The grain size of copper films that were annealed (either before or after the films were subjected to CMP) was not observed to significantly increase over time.

The grain size of the copper in its as-deposited state is affected by the composition of the electroplating bath that is used to electroplate the copper on the substrate. Specifically, it was observed that only baths that contained organic compounds provided copper films with the desired as-deposited grain size (about 0.1 μm to about 0.2 μm). When an acid-based copper sulfate electroplating bath chemistry without organic additives was used, the resulting electroplated copper had an average as-deposited grain size that was too large to provide the desired fill. Although applicants do not wish to be held to a particular theory, it is applicants' belief that electroplated copper films with the desired as-deposited small grain size are only obtained when copper electroplating bath chemistries that contain organic compounds (as either ligands, brighteners, leveling agents, etc.) are used.

What is claimed is:

1. A process for device fabrication comprising:

forming a layer of a dielectric material on a substrate;

forming at least one recess in the layer of dielectric material;

filling the recess in the dielectric material with electroplated copper wherein the electroplated copper has an average grain size of about 0.1 μm to about 0.2 μm; and

annealing the substrate at conditions that increase the average grain size of the electroplated copper to at least 1 μm in at least one dimension.

2. The process of claim **1** wherein the substrate is annealed at a temperature in the range of about 100° C. to about 400° C. for a duration of about one minute to about one hour.

3. The process of claim **1** wherein a barrier layer is formed in the recess before the copper is electroplated onto the substrate.

4. The process of claim **3** wherein a seed layer is formed over the barrier layer before the copper is electroplated onto the substrate.

5. The process of claim **4** wherein the seed layer is formed over the recess.

6. The process of claim **1** further comprising selectively removing a portion of the electroplated copper leaving only the electroplated copper in the recess.

7. The process of claim **1** wherein the recess has a length, a width, and a height.

8. The process of claim **7** wherein the average grain size after anneal is at least as wide as the recess and at least one micron in the length direction of the recess.

9. The process of claim **1** wherein the copper is electroplated from an electroplating bath comprising copper and at least one organic compound.

* * * * *

US006171960B1

(12) **United States Patent**
Lee

(10) **Patent No.: US 6,171,960 B1**
(45) **Date of Patent: Jan. 9, 2001**

(54) **METHOD OF FABRICATING COPPER INTERCONNECTION**

(75) Inventor: **Ellis Lee**, Taipei (TW)

(73) Assignee: **United Microelectronics Corp.**, Hsin-Chu (TW)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/057,812**

(22) Filed: **Apr. 9, 1998**

(30) **Foreign Application Priority Data**

Feb. 6, 1998 (TW) 87101560

(51) **Int. Cl.**[7] **H01L 21/44**

(52) **U.S. Cl.** **438/687**; 438/629; 438/630; 438/658

(58) **Field of Search** 438/687, 664, 438/658, 628, 629, 630

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,447,887 * 9/1995 Filipiak 438/687

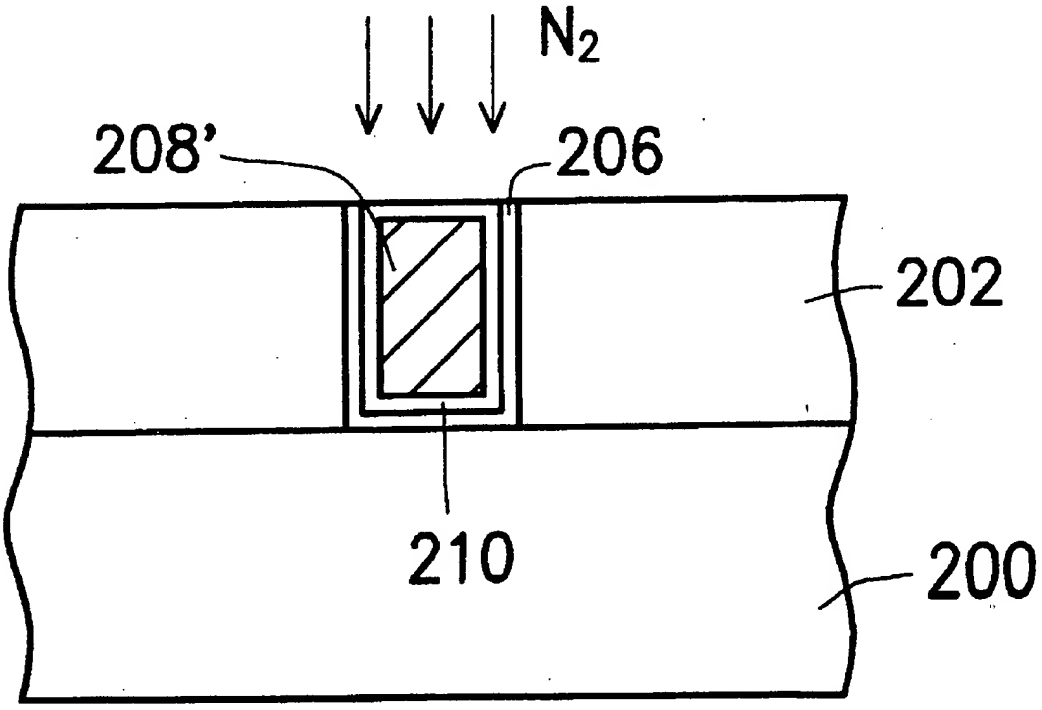
* cited by examiner

Primary Examiner—Caridad Everhart
(74) *Attorney, Agent, or Firm*—Thomas, Kayden, Horstemeyer & Risley

(57) **ABSTRACT**

A method of fabricating copper interconnection is provided comprising forming a dielectric layer with a trench or a via on a semiconductor substrate. A titanium layer is formed on the dielectric layer. A copper layer doped with light silicon is formed in the trench or the via. The copper layer is encapsulated by annealing to make silicon doped in the copper layer diffuse toward the surface of the copper to react with the titanium layer and the gas. It prevents the copper layer from oxidation and diffusion to increase the yield.

15 Claims, 4 Drawing Sheets



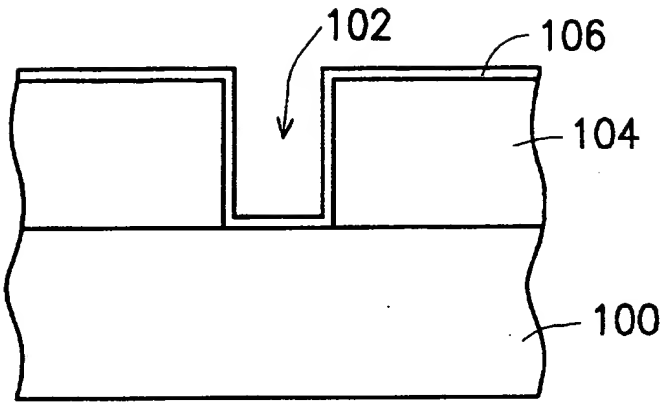


FIG. 1A (PRIOR ART)

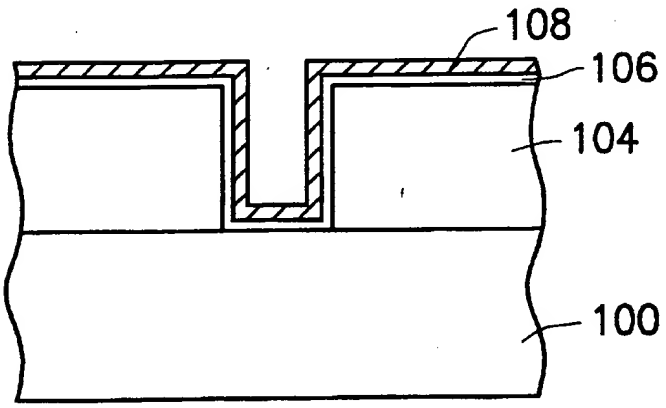


FIG. 1B (PRIOR ART)

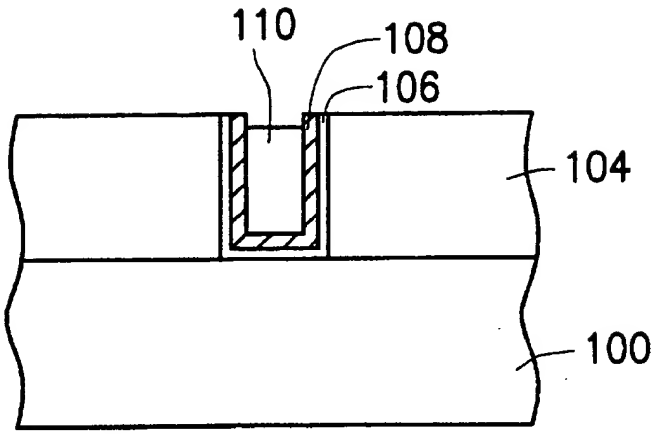


FIG. 1C (PRIOR ART)

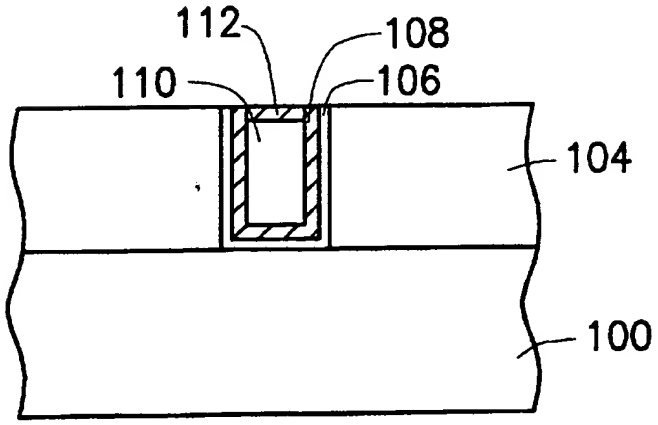


FIG. 1D (PRIOR ART)

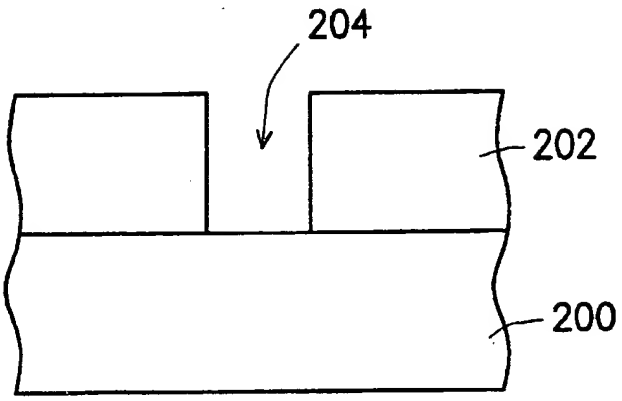


FIG. 2A

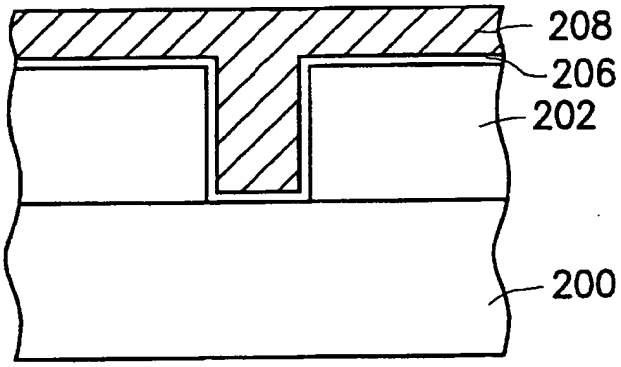


FIG. 2B

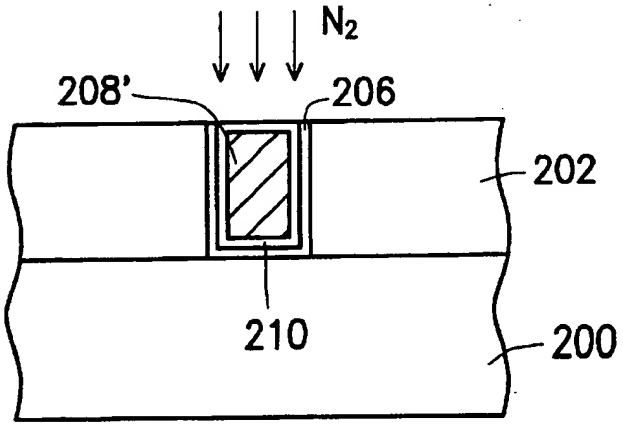


FIG. 2C

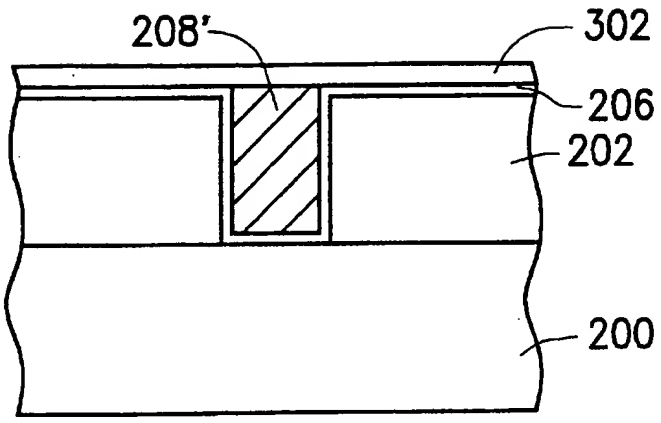


FIG. 3A

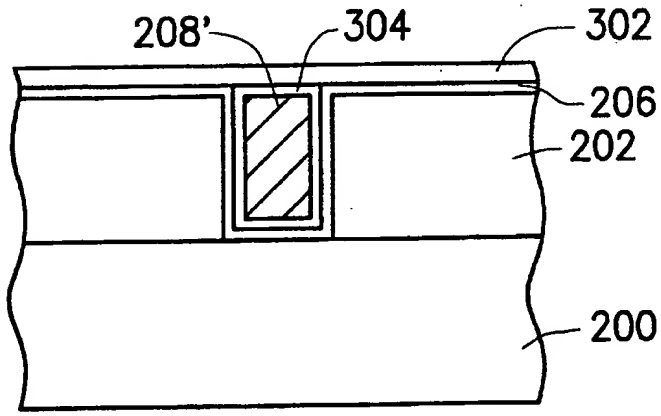


FIG. 3B

METHOD OF FABRICATING COPPER INTERCONNECTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates in general to ultra scale integrated circuits, and more particularly to a method of fabricating copper interconnects in ultra scale integrated circuits.

2. Description of the Related Art

The fabrication of deep submicron ultra large scale integrated (ULSI) circuits requires long interconnects having small contacts and small cross-sections. To achieve the above objectives, the preferred interconnect material is copper. Copper provides a number of advantages for wiring applications including low resistivity and a high melting point.

At present, aluminum is the material used in fabricating interconnects on most integrated circuits. This invention seeks to replace the aluminum with copper in the fabrication of advanced circuits and ultra-fast logic devices.

Many problems, however, are encountered in fabricating circuit interconnects with copper. Some of the major difficulties include: (a) copper oxidizes easily at low temperatures; (2) copper has poor adhesion to substrates; (3) copper diffuses into silicon dioxide and other dielectric material used in micro-circuitry; and (4) copper requires a high temperature for patterning by reactive ion etching.

In order to overcome these disadvantages when using copper as an interconnect material, it is necessary to passify the copper surfaces and provide diffusion barriers between the copper and the adjacent layers. A layer of titanium nitride (TiN) has been suggested as a possible diffusion barrier due to its inert and conductive nature.

FIGS. 1A–1D are cross-sectional views showing a conventional method of fabricating copper interconnects. Referring to FIG. 1A, a semiconductor substrate **100** is provided. A dielectric layer **104** with a via **102** is formed on the semiconductor substrate **100**. A titanium layer **106** is formed, for example, by sputtering in the via **102** and on the dielectric layer **104** under argon gas. The titanium layer **106** has a thickness of about 200–500 Å.

Referring to FIG. 1B, a first titanium nitride layer **108** is formed, for example, by nitriding under N_2 gas or NH_3 gas at high temperature on the titanium layer **106** as a adhesion layer.

Referring to FIG. 1C, a copper layer **110** is formed on the first titanium nitride layer **108**. Excess copper material outside of the via **102** is removed by chemical mechanical polishing to expose the semiconductor substrate **100**.

Referring to FIG. 1D, a second titanium nitride layer **112** is formed on the copper layer **110** to avoid the oxidation and preserve the characters of the interconnections. The process of fabricating copper interconnects described above provides a copper layer in the via as an interconnect. A titanium layer and a titanium nitride layer are deposited between the copper layer and other dielectric layers as a barrier layer and an adhesion layer to protect the copper layer from oxidation and prevent it form diffusing.

A number of limitation to the above method have been discovered, however, particularly when forming fully-planar copper lines by filling grooves in a dielectric and removing the excess. In this case, the copper must be deposited into a feature without leaving a void, so electroplating or chemical vapor deposition is required. It is difficult to deposit refractory copper or metal-copper alloys, such as copper-titanium, with electroplating or chemical vapor deposition techniques.

SUMMARY OF THE INVENTION

It is therefore the object of the invention to provide an improved and simplified method of fabricating copper interconnects. The present invention skips the step of depositing a barrier layer. An impurity doped in the copper layer diffuses toward the surface of the copper layer and reacts with the titanium or a gas to form the barrier layer. The method reduces the cost and the steps to form the barrier layer.

The invention achieves the above-identified objects by providing one new method of fabricating copper interconnection. First, a semiconductor substrate with a trench or a via is provided. A titanium layer is form as a barrier layer on the semiconductor substrate. A copper layer doped with light silicon is formed in the trench or the via. The excess of the copper layer is removed by CMP to expose the surface of the semiconductor substrate. The copper layer is annealed under nitrogen gas to make silicon doped in the copper layer diffuse toward the surface of the copper layer. Silicon reacts with the titanium layer and nitrogen gas to form a silicon nitride layer and a titanium silicide layer to encapsulate the copper layer.

The invention achieves the above-identified objects by providing another new method of fabricating copper interconnection. First, a semiconductor substrate with a trench or a via is provided. A titanium layer is formed as a barrier layer on the semiconductor substrate. A copper layer doped with light silicon is formed in the trench or the via. The excess of the copper layer is removed by CMP to expose the surface of the semiconductor substrate. Then, a second titanium layer is formed on the copper layer. The copper layer is annealed under argon gas to make the silicon doped in the copper layer diffuse toward the surface of the copper layer. Silicon reacts with the titanium layer, the second titanium layer forms a titanium silicide layer to encapsulate the copper layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The description is made with reference to the accompanying drawings in which:

FIGS. 1A–1D are cross-sectional views showing a conventional method of fabricating copper interconnects;

FIGS. 2A–2C are cross-sectional views showing the process steps of a first embodiment of the method of fabricating copper interconnects; and

FIGS. 3A–3B are cross-sectional views shoeing the process steps of a second embodiment of the method of fabricating copper interconnects.

DESCRIPTION OF THE PREFERRED EMBODIMENT

First Embodiment

The present invention uses copper as the material for the interconnect lines of a ULSI circuit. Copper was chosen over aluminum for its low bulk electrical resistivity (50% lower than aluminum), and its higher melting temperature (1083° C. versus 600° C.). Copper also exhibits a high electromigration resistance, which greatly improves the reliability of the interconnect lines in functioning properly in the circuit.

If copper is to be used successfully in the ULSI circuit, conformal layers, also referred to as diffusion barriers, are required to prevent the copper from interacting with sur-

rounding materials. The present invention reflects the discovery that copper can be encapsulated with a titanium silicide layer. The titanium silicide layer is used to encapsulate the copper interconnect lines. The interconnect lines of the ULSI circuit exhibit improved thermal stability, higher oxidation resistance, low electrical resistance, and a favorable electromigration lifetime.

Referring first to FIG. 2A, a semiconductor substrate **200** is provided. A dielectric layer **202** is formed on the semiconductor substrate **200**. The material of the dielectric layer is, for example, silicon dioxide formed by chemical vapor deposition (CVD). A trench or a via **204** coupling with the semiconductor substrate **200** is formed in the dielectric layer **202** by photolithography.

Referring to FIG. 2B, a adhesion layer **206** is formed in the via **204** and on the semiconductor substrate **200**. The material of the adhesion layer **206** is, for example, titanium formed by sputtering with a thickness about of 200–500 Å. A copper layer **208** is formed on the adhesion layer **206** and in the via **204**. The copper layer has a impurity of silicon. The concentration of the silicon is about 10 percentage.

Referring to FIG. 2C, the excess of the copper layer **208** out side of the via **204** is removed, for example, by chemical mechanical polishing (CMP) to expose the semiconductor substrate **200** and form a copper line **208'** in the via **204**. The step of annealing is proceeded under nitrogen gas. The step makes the silicon doped in the copper layer diffuse toward the surface of the copper layer and react with the adhesion layer **206** and nitrogen gas to form a silicon nitride layer and a titanium silicide layer **210**. The silicon nitride layer and the titanium silicide layer **210** encapsulate the copper line **208'** to prevent the copper line from oxidation and diffusion.

Second Embodiment:

Referring first to FIG. 3A, after finishing the structure shown in the FIG. 2B in the first embodiment, the excess of the copper layer **208** is removed, for example, by CMP to expose part of the adhesion layer **206** and form a copper line **208'** in the via **204**. Then, a second adhesion layer **302** is formed on the copper line **208'** and the adhesion layer **206**.

Referring to FIG. 3B, a step of annealing is done under argon gas. The step makes the silicon doped in the copper lines **208'** diffuse toward the surface of the copper line **208'**, and react with the adhesion layer **206** and the second adhesion layer to form a titanium silicide layer **304**. The titanium silicide layer **304** encapsulates the copper line to prevent from oxidation and diffusion.

The present invention provides a method using the silicon doped in the copper layer to form a titanium silicide layer by reacting the silicon with titanium in the step of annealing. The titanium silicide layer prevents the copper line from oxidation and diffusion. The present invention is a simple process and reduces the cost.

While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto. To the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. A method of fabricating copper interconnection, comprising the steps of:

providing a semiconductor substrate, wherein the semiconductor substrate at least has a trench or a via;

forming an adhesion layer in the trench or the via and on the semiconductor substrate;

forming a copper layer on the adhesion layer, wherein the copper layer has an impurity of silicon, wherein the impurity of silicon is doped in the copper layer; and

annealing under nitrogen to form a silicide layer encapsulating the copper layer and a silicon nitride layer.

2. A method according to claim **1**, wherein the adhesion layer is a metal layer.

3. A method according to claim **2**, wherein a material of the metal layer is titanium or tantalum.

4. A method according to claim **1**, wherein the copper layer having an impurity of silicon and the adhesion layer are partially removed to expose the surface of the semiconductor substrate before the step of annealing under nitrogen gas.

5. A method according to claim **4**, wherein the step of partially removing the copper layer having a impurity with silicon is done by chemical mechanical polishing.

6. A method according to claim **4**, wherein the silicon doped in the copper layer is about 10 percentage.

7. A method of fabricating copper interconnection, comprising the step of:

providing a semiconductor substrate, wherein the semiconductor substrate at least has a trench or a via;

forming a first adhesion layer in the trench or the via;

forming a copper layer with a impurity of silicon on the first adhesion layer;

partially removing the copper layer with a impurity of silicon and the first adhesion layer to expose the semiconductor substrate, wherein the impurity of silicon is doped in the copper layer;

forming a second adhesion layer on the copper layer with an impurity of silicon and the semiconductor substrate; and

annealing under argon gas to form a silicide layer encapsulating the copper layer.

8. A method according to claim **7**, wherein the first adhesion layer is a metal layer.

9. A method according to claim **8**, wherein the material of the metal layer is titanium or tantalum.

10. A method according to claim **7**, wherein the silicon doped in the copper layer is about 10 percentage.

11. A method according to claim **7**, wherein the second adhesion layer is a metal layer.

12. A method according to claim **11**, wherein the material of the metal layer is titanium or tantalum.

13. A method according to claim **7**, wherein the step of partially removing the copper layer with a impurity of silicon and the first adhesion layer to expose the semiconductor substrate is done by chemical mechanical polishing.

14. A method of fabricating copper interconnection, comprising the steps of:

proving a semiconductor substrate;

forming a trench or a via on the semiconductor substrate;

forming a titanium layer in the trench or the via and on the semiconductor substrate;

forming a copper layer with a impurity of silicon on the titanium layer, wherein the impurity of silicon is doped in the copper layer;

partially removing the copper layer with an impurity of silicon to expose the semiconductor substrate; and

annealing under nitrogen gas to form a titanium silicide layer encapsulating the copper layer and a silicon nitride layer.

15. A method according to claim **14**, wherein the silicon doped in the copper layer is about 10 percentage.

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